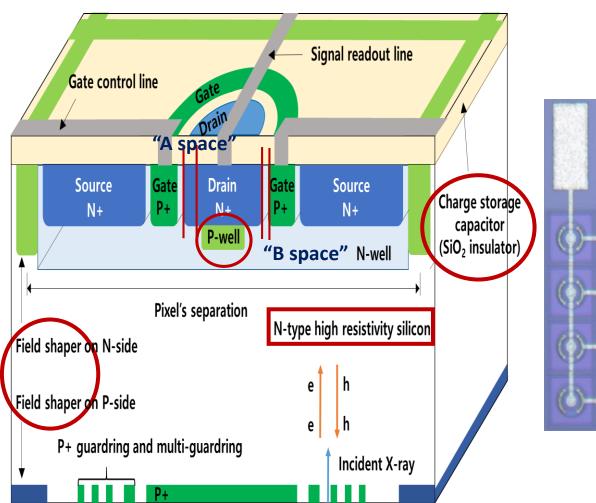
Switch Performance Measurement of Junction Field Effect Transistor Integrated in Pixel Sensor

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Design concept of pixelated silicon PIN sensors with JFET structure



Pixel size: 200, 100, 30 um

• **PIN structure**: for the detection efficiency for low energy X-ray

Drain

Gate

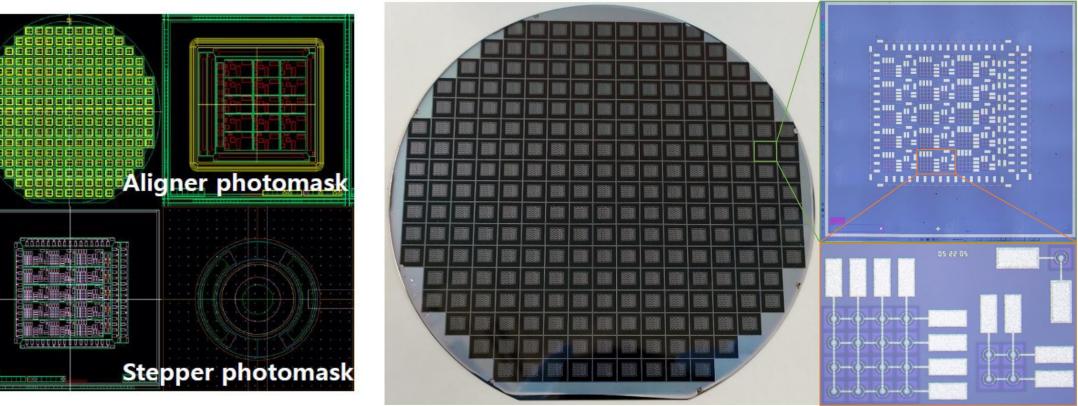
- high resistivity (>5 k Ω ·cm) N-type 650 μ m thick, 6 in. silicon wafer

Cylindrical JFET structure
switch off : by applying a reverse bias voltage to the gate
switch on : charges are transferred from the source to the drain

- all pixels within one row are read in parallel and the next row is then selected by the control voltage after the previous row's is finished

Fabrication

- Design parameters for fabrication
- P-well doping: 7.0, 7.5, 8.0x10¹³ cm⁻²
- A space: 0.5, 1.0, 1.4 μm
- B space: 1.4, 1.8, 2.2 μm
- C and D spaces: 0, 5, 10 μm



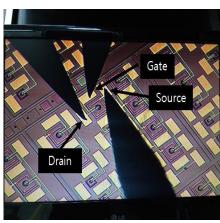
- 1 stepper photomask (6 layer patterns) and 5 aligner photomask
- One of the fabricated wafers on 6-in. wafers with 25 different designs
- Electronics and Telecommunications Research Institute (ETRI) in Korea

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8.2 mm x 7.7 mm

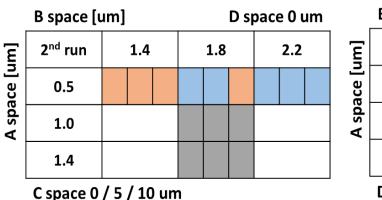
Switch Performance Test

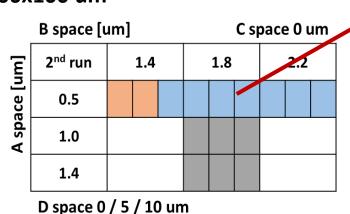




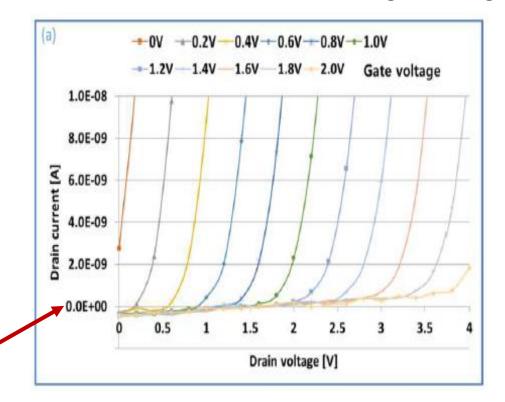
For electrical characteristic measurements

Pixel size: 100x100 um²





I–V characteristics of a JFET for various gate voltages



As expected, the larger the drain voltage at a given gate voltage, the larger the drain current, and the larger the gate voltage, the smaller the drain current.

Summary

- Pixelated silicon sensors with a cylindrical JFET structure were fabricated
- We determined design parameters showing good switching function

 switching efficiency is improved with a decrease in the JFET size,
 and with increases in the A and B space values.
 - switch-off resistance of the JFET was found to reach about $10^{10} \Omega$
 - Although this value appears to be relatively low, the switching functioned well for a gate voltage between -1 and -2 V.