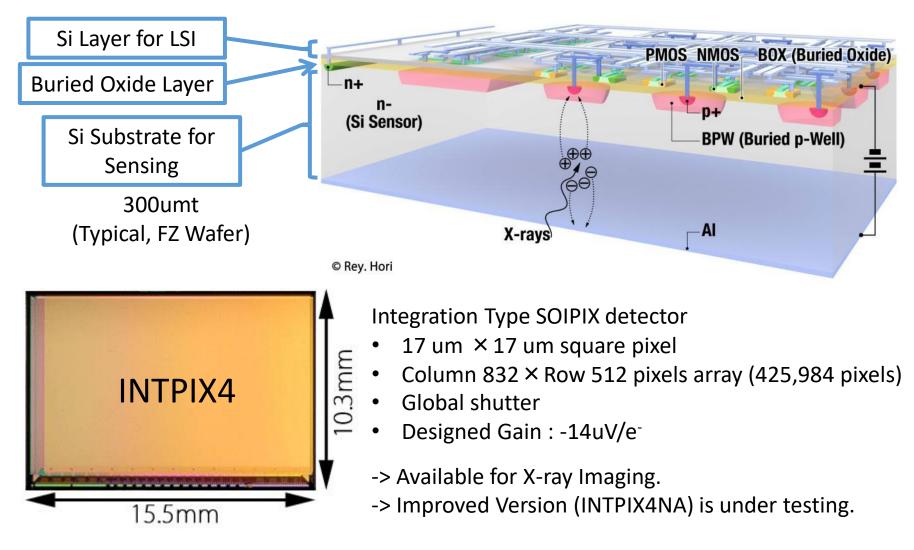


Development status of new readout system for SOI pixel detector using 10 Gb Ethernet SiTCP

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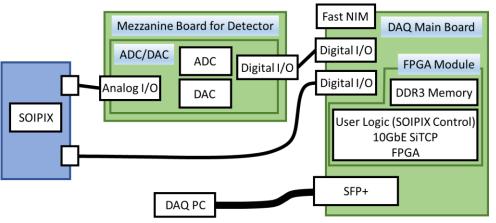
SOI pixel detector (SOIPIX)



New readout system using 10GbE SiTCP

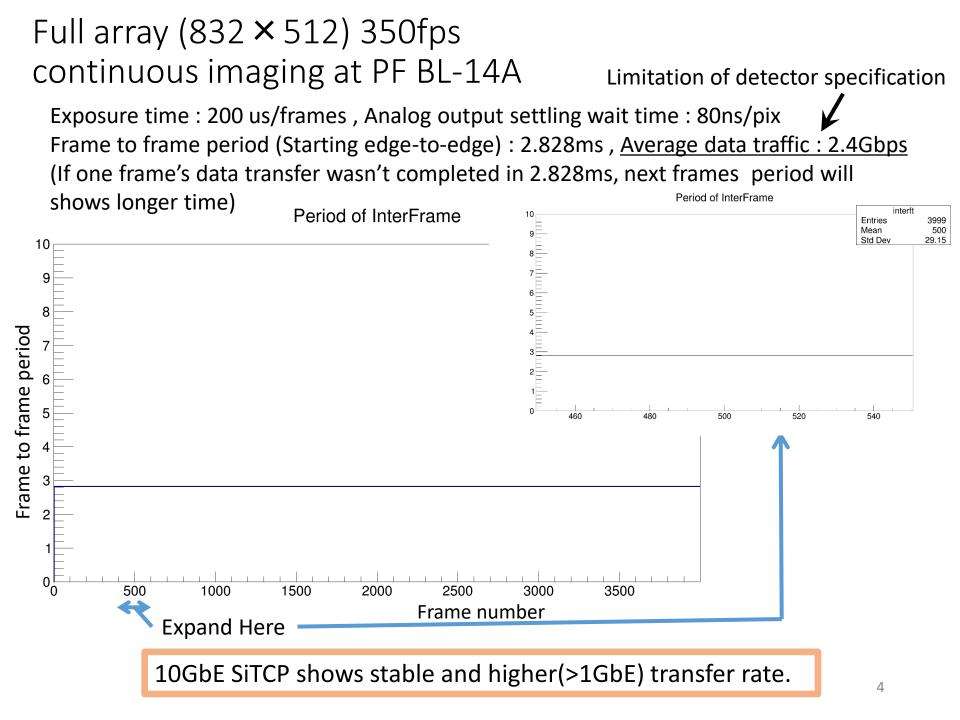
<u>SiTCP</u> is a network processor IP (Intellectual Property) core that can be implemented in an FPGA.

- Developed by Tomohisa Uchida (KEK ESYS), and currently developed and supported by Bee Beans Technologies.
- Small circuit size(~3000 Slice), simple FIFO like I/F, close to specification maximum transfer speed caused by Hardware-based implementation and easy to customize.
- Present system using 1GbE SiTCP, and it is not enough for advanced experiments. (high framerate, large area etc.)
- -> 10GbE SiTCP (SiTCP-XG) is upgrade version of SiTCP and strong solution for our readout system.

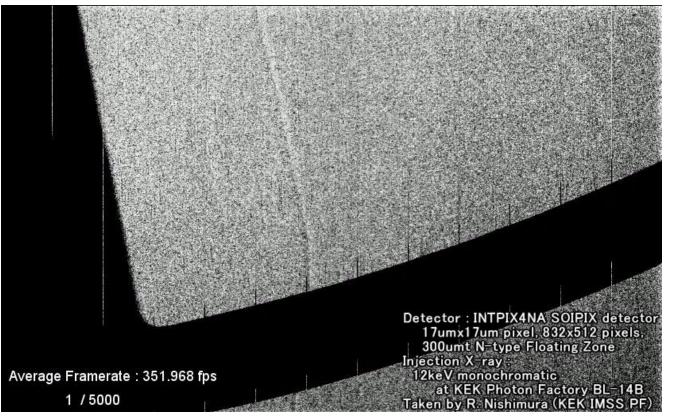


10GbE SiTCP readout system

- New readout boards (pilot production) were developed and now under testing.
- 10GbE SiTCP was implemented to Kintex-7 FPGA, mixed implementation with SOIPIX control logic.
- Prototype of new system was developed on KC705 commercial FPGA evaluation board with Alpha release of 10GbE SiTCP. (Results were shown in next slides)



Full array (832 × 512) 350fps continuous imaging at PF BL-14B



Sample : 12keV X-ray Profile with Optical Chopper Exposure time : 200 us/frames , Analog output settling wait time : 80ns/pix. (Same as previous BL-14A result slide)

This is the initial result of SOIPIX X-ray imaging data with 10GbE SiTCP. 10GbE SiTCP was advanced to Beta release and now you can try! (https://github.com/BeeBeansTechnologies/SiTCPXG_Netlist_for_Kintex7)