AZImuthal INTegration for fast X-ray area detectors on FPGAs

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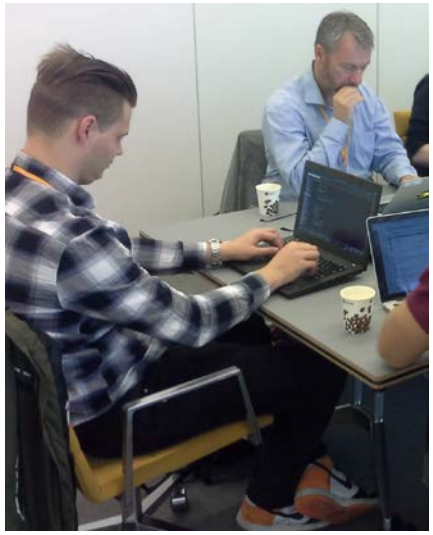
Carl and Brian – both NBI, Carl is a phd student in *X-ray imaging applications for food industry* project and Brian is an e-Science professor at NBI



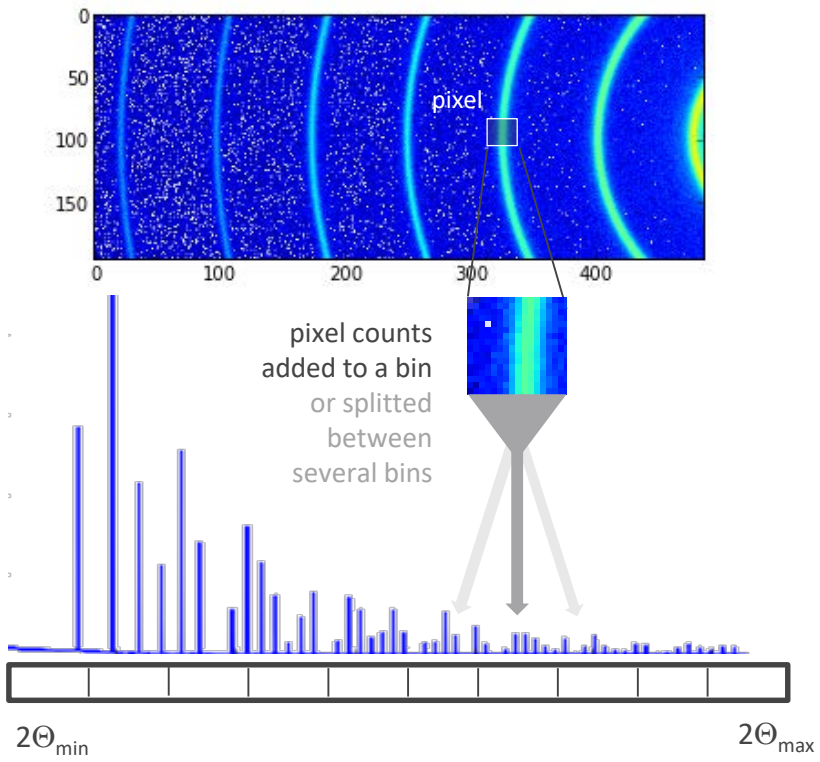
*SME: Synchronous Message Exchange: https://sme-hdl.org

Azimuthal integration

why on FPGA ?

1st Simple problem: binning

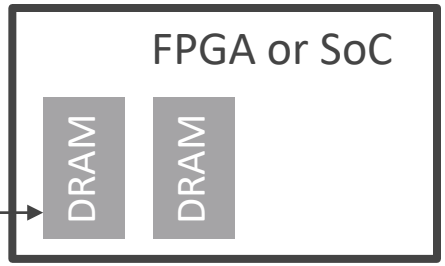
- data reduction: ~1 Mpix -> ~1k bins



2nd Scientific part can be separeted

- easy for ”static” detectors
- non-integer arithmetic needed for scientific accuracy
- pixel-bin “routing/mapping” as well as real value weights and pixel corrections can be calculated in advance and stored in device memory (high throughput -> requirements on dev-mem)

custom cpu sw,
matFRIA, pyFA,
...
--->
configuration
(many bytes per
pixel)

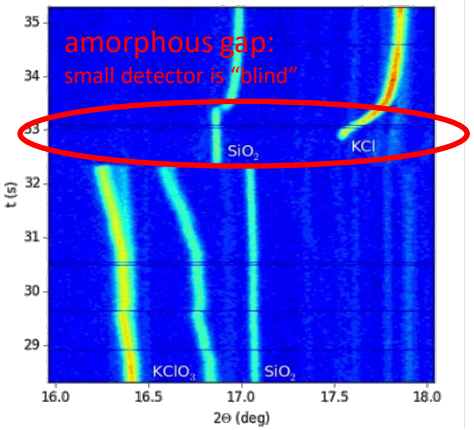


Azimuthal integration

on FPGA ?!

3rd Real-time x-ray probe as trigger for slower detectors

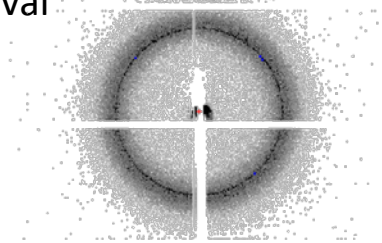
fast but small detector
with limited Q-rage



large but slow

4th binning/histograming/AZINT – important algorithms

- crystallography:
  - background estimation
  - ice-ring removal
- . . .

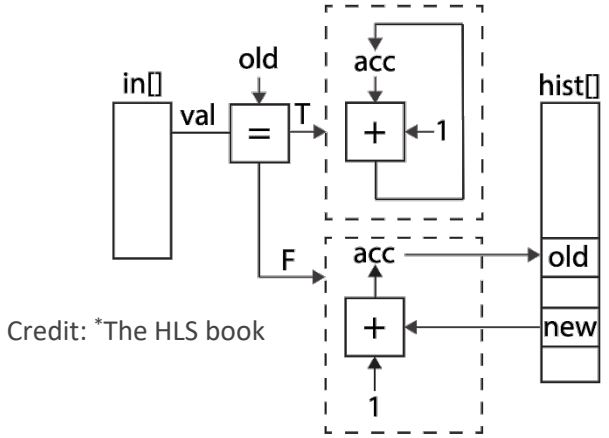


n-th non-synchrotron

- portable instruments
- space applications:
  - limitted bandwidth for data transfer
  - energy efficiency

Azimuthal integration

FPGA implementation



Credit: *The HLS book

- a simple 3 stage pipeline at FPGA
  - ref: PREFIX SUM AND HISTOGRAM in Kastner, Matai, Neuendorffer: *Parallel *Programming for FPGAs - the HLS book*, http://kastner.ucsd.edu/hlsbook/
- in HLS can be fully pipelined
- initial implementation in SME: github.com/bh107/SME-Binning
  - Xilinx Zynq Z7020 at 100 MHz: 1 Gpix/s (10% util. per processing unit)
  - Xilinx Kintex Ultrascale+ xcku5p at 590 MHz: 20 Gpix/s (3% util. per unit)
- floating point:
  - single loop with HLS + bitonic-merge
  - with OpenCL: gitlab.maxiv.lu.se/compute-fpgas
- note: result stored in BRAM, often high *nbins* (~10k) required which can be also limiting factor

Azimuthal integration

AZINT – FPGA accelerated Azimuthal integration with OpenCL/SME

- figures:
  - Nallatech 385A – Intel Aria10: medium size FPGA (20 nm)
  - processing pipelines: 32 (fp32, double possible, 8k nbins)
  - host-to-device data transfer: 4.6 GB/s – can handle 4M x 500 Hz
  - 5.8 Gpix/s – allows average pixel-splitting=3 for 4M x 500 Hz
  - comparable to NVIDIA V100 (~ 6 Gpix/s)
- TODO:
  - optimizations for Stratix10 FPGAs (and OneAPI)
  - OpenCL -> HLS/SME
    - cost and energy optimized Xilinx boards: Zynq Z7020
    - large Xilinx Ultrascale+ with 100Gbs MAC