

AZImuthal INTegration for fast X-ray area detectors on FPGAs



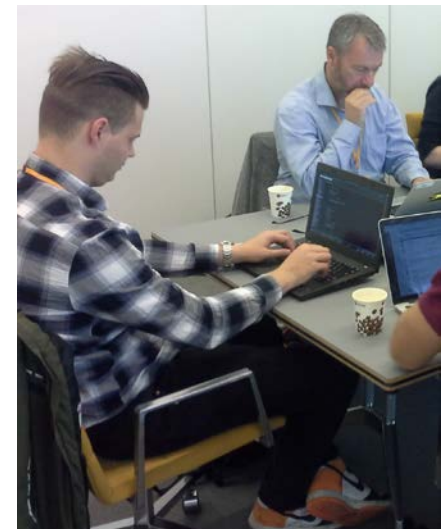
Artur – physics, CERN,
MAX IV network and
infrastructure team

Kenneth – expert in FPGA
languages, ‘inventor’ of SME*,
assistant prof. at NBI
former eSCIENCE postdoc at
MAX IV



Zdenek – MAX IV
scientific sw, x-ray
scattering data
processing

Carl and Brian – both NBI,
Carl is a phd student in
*X-ray imaging applications
for food industry* project
and Brian is an e-Science
professor at NBI



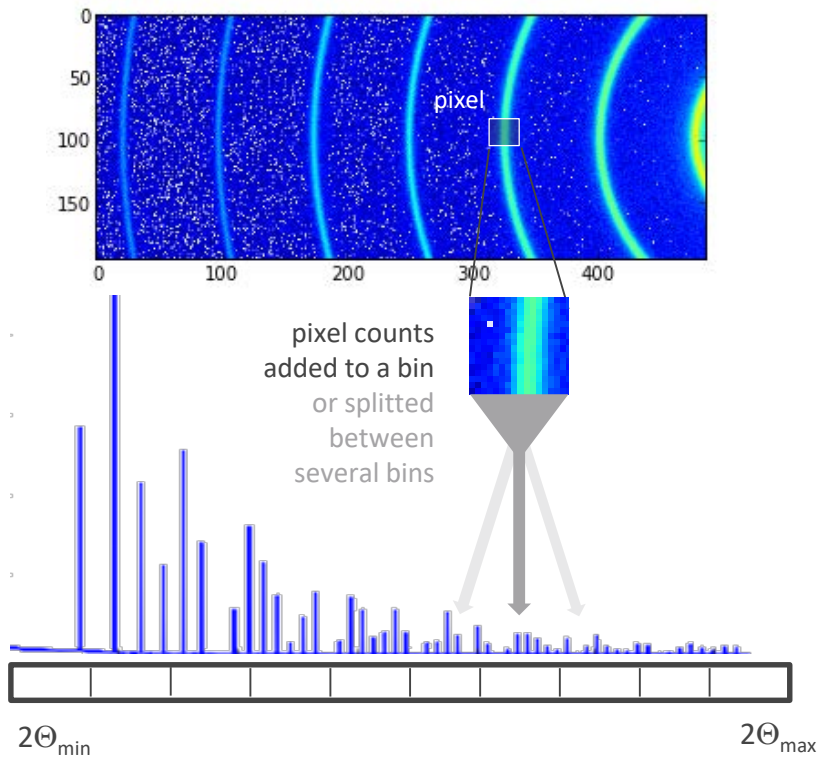
*SME: Synchronous Message Exchange: <https://sme-hdl.org>

Azimuthal integration

why on FPGA ?

1st Simple problem: binning

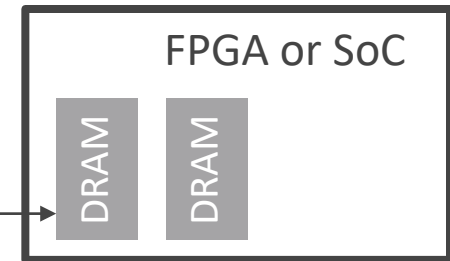
- data reduction: ~ 1 Mpix \rightarrow ~ 1 k bins



2nd Scientific part can be separated

- easy for "static" detectors
- non-integer arithmetic needed for scientific accuracy
- pixel-bin "routing/mapping" as well as real value weights and pixel corrections can be calculated in advance and stored in device memory (high throughput \rightarrow requirements on dev-mem)

custom cpu sw,
matFRIA, pyFA,
...
--->
configuration
(many bytes per pixel)

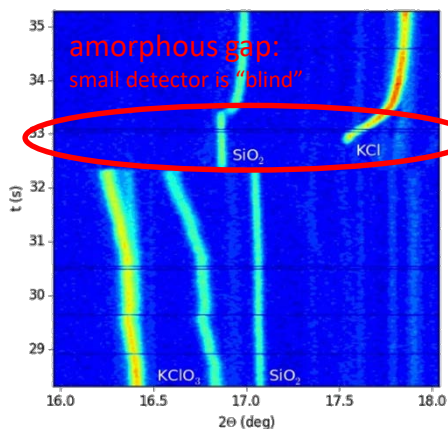
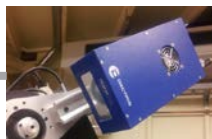


Azimuthal integration

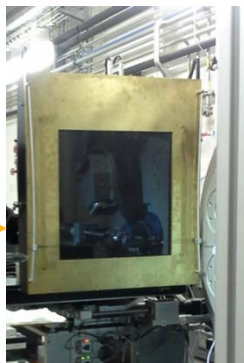
on FPGA ?!

3rd Real-time x-ray probe as trigger for slower detectors

fast but small detector with limited Q-range

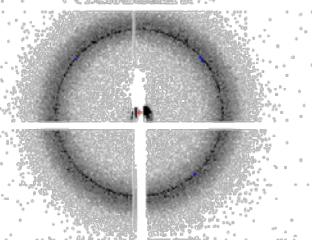


large but slow



4th binning/histogramming/AZINT – important algorithms

- crystallography:
 - background estimation
 - ice-ring removal
- ...

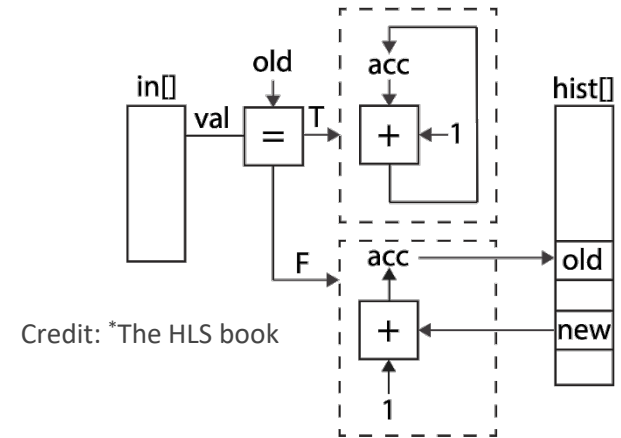


nth non-synchrotron

- portable instruments
- space applications:
 - limited bandwidth for data transfer
 - energy efficiency

Azimuthal integration

FPGA implementation



- a simple 3 stage pipeline at FPGA
 - ref: PREFIX SUM AND HISTOGRAM in Kastner, Matai, Neuendorffer: *Parallel *Programming for FPGAs - the HLS book*, <http://kastner.ucsd.edu/hlsbook/>
- in HLS can be fully pipelined
- initial implementation in SME: github.com/bh107/SME-Binning
 - Xilinx Zynq Z7020 at 100 MHz: 1 Gpix/s (10% util. per processing unit)
 - Xilinx Kintex Ultrascale+ xcku5p at 590 MHz: 20 Gpix/s (3% util. per unit)
- floating point:
 - single loop with HLS + bitonic-merge
 - with OpenCL: gitlab.maxiv.lu.se/compute-fpgas
- note: result stored in BRAM, often high *nbins* (~10k) required which can be also limiting factor

Azimuthal integration

AZINT – FPGA accelerated Azimuthal integration with OpenCL/SME



```
[main] start
[main] --- Test data ---
[main] cols: [ 0 1 2 ... 4500093 4500094 4500095 ]
[main] rows: [ 1 2 3 ... 1125024 1125024 1125024 ]
[main] cor[:5]: [ [1. 0.5 0.33333334 0.25 0.2 ] ]
[main] wgt[:5]: [ [1. 1. 1. 1. 1.] ]
[main] dta1[0,:]: [ 1 2 3 ... 43646 43647 43648 ]
[main] --- Reference integration ---
[main] bin[:0]: [ [49671.387 49672.336 49673.266 ... 0. 0. 0. ] ]
[main] ncs[:0]: [ [1125024. 1125024. 1125024. ... 0. 0. 0.] ]
[azint-cl] OpenCL will use AOCX binary image: /mxn/groups/pub/sw/fpga/bin/p385a_mac_ax115/azint_demo_uint16_float_p32b128_no
Reprogramming device [0] w1 w2 ktp1 ktp2 kai write1 write2 transpose1 transpose2
[azint-cl] time time time time time start end start end start end start end effect
[azint-cl] (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) (ms) %
[azint-cl] 23.1 23.2 27.5 27.5 25.0 50.93 74.08 78.21 110.82 78.13 112.06 112.19 139.67 78.12 98.25
[azint-cl] 23.2 32.6 33.9 27.5 25.0 50.93 74.08 78.21 110.82 78.13 112.06 112.19 139.67 164.66 98.26
[azint-cl] 23.1 32.6 33.9 27.5 24.9 235.96 259.05 263.39 295.94 263.32 297.26 297.50 324.97 201.89 98.30
[azint-cl] 23.1 32.5 33.9 27.5 24.9 235.96 259.05 263.39 295.94 263.32 297.26 297.50 324.97 201.89 98.27
[azint-cl] 23.1 32.5 33.9 27.5 24.9 235.96 259.05 263.39 295.94 263.32 297.26 297.50 324.97 325.00 98.31
[azint-cl] 23.1 32.5 33.9 27.5 24.9 297.61 320.69 325.07 357.62 324.99 358.92 358.94 386.42 386.45 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 420.70 443.74 448.16 480.69 448.07 482.00 482.01 509.48 448.09 98.29
[azint-cl] 23.0 32.5 33.9 27.5 24.9 420.70 443.74 448.16 480.69 448.07 482.00 482.01 509.48 509.52 98.30
[azint-cl] 23.0 32.5 33.9 27.5 24.9 482.55 510.19 518.76 542.12 509.50 543.44 543.60 571.07 571.11 98.32
[azint-cl] 23.1 32.5 33.9 27.5 24.9 605.18 628.22 632.61 665.16 632.53 666.47 666.63 694.10 694.14 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 605.18 628.22 632.61 665.16 632.53 666.47 666.63 694.10 694.14 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 666.75 689.79 694.21 726.74 694.12 728.07 728.08 755.55 755.59 98.27
[azint-cl] 23.0 32.5 33.9 27.5 24.9 728.22 751.26 755.65 788.18 755.57 789.52 789.66 817.13 817.17 98.30
[azint-cl] 23.0 32.5 33.9 27.5 24.9 789.79 812.81 817.24 849.77 817.15 851.09 851.11 878.58 878.62 98.25
[azint-cl] 23.1 32.5 33.9 27.5 24.9 851.26 874.31 878.68 911.22 878.60 912.52 912.70 940.17 940.21 98.26
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1001.21 1030.24 1030.24 1061.72 1061.72 1097.14 1097.14 1124.66 1124.70 98.27
[azint-cl] 23.1 32.5 33.9 27.5 24.9 1035.86 1058.91 1063.32 1095.85 1063.22 1097.17 1097.19 1124.66 1124.70 98.27
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1035.86 1058.91 1063.32 1095.85 1063.22 1097.17 1097.19 1124.66 1124.70 98.27
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1124.77 1157.30 1124.68 1158.62 1158.79 1186.27 1186.31 1211.25 1186.31 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1186.38 1218.92 1186.29 1220.22 1220.24 1247.72 1247.76 1272.70 1247.76 98.29
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1220.43 1243.46 1247.83 1280.38 1247.74 1281.68 1281.87 1309.34 1309.38 98.24
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1343.47 1366.51 1370.90 1403.43 1370.80 1404.73 1404.91 1432.38 1432.42 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1343.47 1366.51 1370.90 1403.43 1370.80 1404.73 1404.91 1432.38 1432.42 98.28
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1466.34 1493.82 1466.34 1493.82 1466.34 1493.82 1493.82 1518.80 1493.82 98.29
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1528.12 1551.15 1555.56 1588.09 1555.46 1589.40 1589.41 1616.89 1616.93 98.27
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1589.59 1612.64 1617.00 1649.52 1616.91 1650.84 1651.01 1678.48 1678.52 98.29
[azint-cl] 23.0 32.5 33.9 27.5 24.9 1651.16 1674.18 1678.60 1711.13 1678.50 1712.43 1712.45 1739.93 1739.96 98.29
[azint-cl] 23.1 32.5 33.9 27.5 24.9 1712.64 1735.70 1740.04 1772.57 1739.94 1773.89 1774.06 1801.53 1801.57 98.26
[azint-cl] 23.0 32.5 33.9 27.5 24.6 1774.21 1797.23 1801.65 1834.18 1801.55 1835.48 1835.50 1862.97 1862.99 99.44
[azint-cl] (task-average) wrate1 = 6246.9 (MB/s), wrate2 = 4468.7 (MB/s), trate1 = 4270.4 (MB/s), trate2 = 5241.3 (MB/s), vpixrate = 5.775 (Gpix/s)
[azint-cl] (full-average) tm = 1.888 (sec), ntasks = 30, rate = 4575.4 (MB/s), vpixrate = 2.288 (Gpix/s)
[main] --- OpenCL integration ---
[main] bin[:0]: [ [49671.387 49672.336 49673.266 ... 0. 0. 0. ] ]
[main] ncs[:0]: [ [1125024. 1125024. 1125024. ... 0. 0. 0.] ]
[main] Test passed: True
```

● figures:

- Nallatech 385A – Intel Aria10: medium size FPGA (20 nm)
- processing pipelines: 32 (fp32, double possible, 8k nbins)
- host-to-device data transfer: 4.6 GB/s – can handle 4M x 500 Hz
- 5.8 Gpix/s – allows average pixel-splitting=3 for 4M x 500 Hz
- comparable to NVIDIA V100 (~6 Gpix/s)

● TODO:

- optimizations for Stratix10 FPGAs (and OneAPI)
- OpenCL -> HLS/SME
- cost and energy optimized Xilinx boards: Zynq Z7020
- large Xilinx Ultrascale+ with 100Gbs MAC