XIDER: a novel X-ray detector for the next generation of high-energy synchrotron radiation sources

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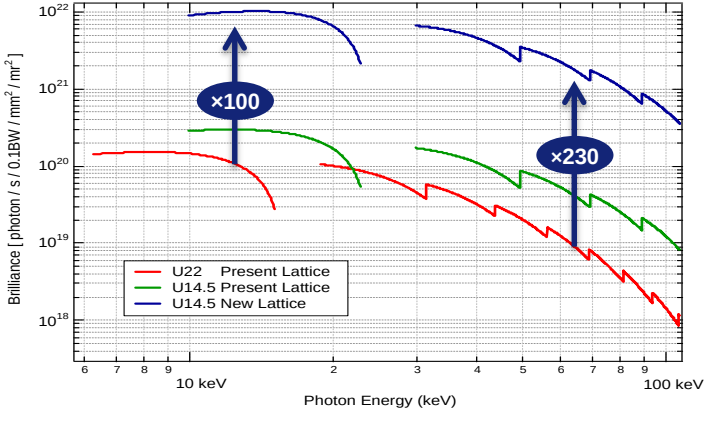
On behalf of the XIDER collaboration

THE 4TH GENERATION SYNCHROTRON CHALLENGES

The Extremely Bright Source (ESRF-EBS)

- First worldwide high-energy 4th generation synchrotron facility. Other facility upgrades ongoing or planned
- Two main challenges:
  1. ×100 more brilliant: high-flux
  2. High-energy X-rays
- New X-ray instrumentation required to exploit the new source

Brilliance



The XIDER project

- R&D feasibility study (2019-2023)
  - Collaboration with Heidelberg University for microelectronic design

ESRF
The European Synchrotron

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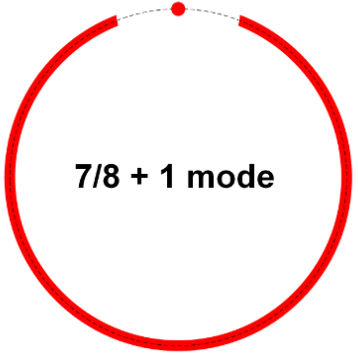
THE XIDER PROJECT

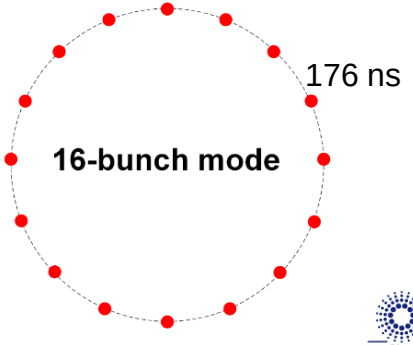
XIDER: Very fast high dynamic range digital integrating detector at **storage rings**

- 2D hybrid pixel detector for **high energy** and **time-resolved** diffraction experiments with ESRF-EBS
- Based on the novel **incremental digital integration** read-out scheme
- Main targets:
  - ✓ Design optimised to operate with high-Z sensors (**30-100 keV**)
  - ✓ 100 µm target pixel pitch (**configurable** 2×2 **binning**)
  - ✓ High photon fluxes (**up to 10^9** photons/second/pixel)
  - ✓ **Time resolved** capability: burst mode up to 5.68 Mframes/s
  - ✓ High duty cycle, deadtime free readout
  - ✓ **Fully digital** readout

Continuous mode
(high flux)



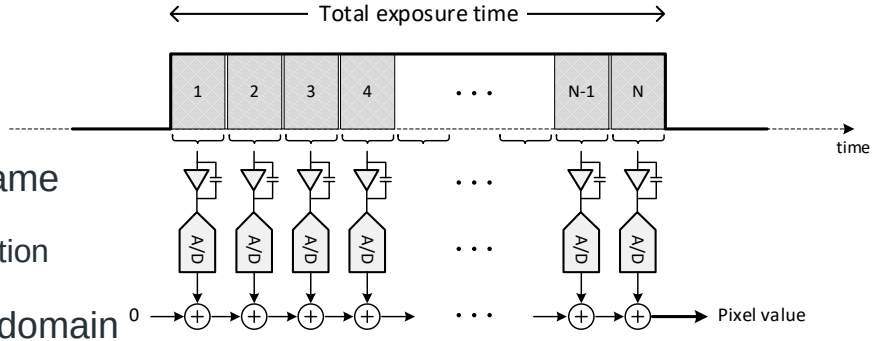
Pulsed mode
(time resolved)



THE INCREMENTAL DIGITAL INTEGRATION

Incremental digital integration:

1. The total exposure time is divided in µs subframes
2. The signal is integrated and digitised for each subframe
   - Noise and leakage are suppressed by signal quantisation
3. The subframe values are accumulated in the digital domain
   - All this processing happens ‘in the pixel’



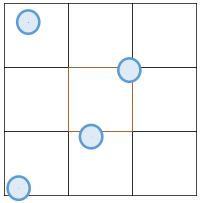
Readout scheme discussed in: *J. Inst.* **15** C01040
https://doi.org/10.1088/1748-0221/15/01/C01040

Interesting practical advantages:

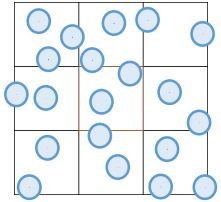
- Suppression of leakage current contributions
- Provides single photon sensitivity
- High dynamic range is achievable
- Fully digital readout
- High resolution ADCs not required

Main challenges of this new readout scheme:

- Minimise the effects of partial charge collection (space and time)
- Combine low-flux and high-flux regimes



Low flux (PC)



High flux (CI)

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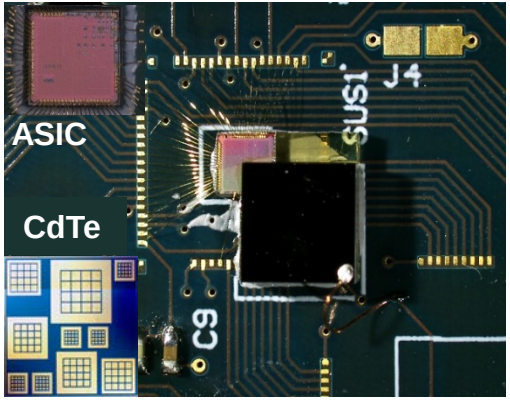
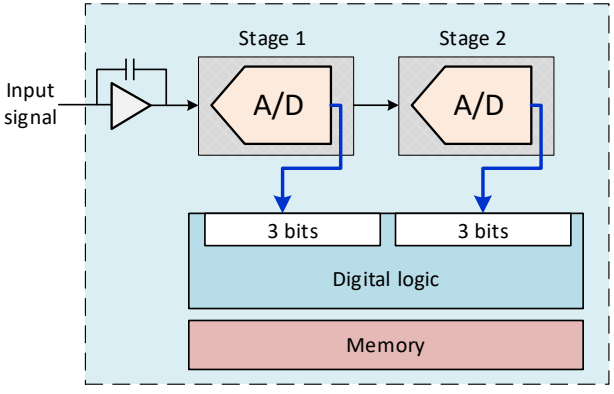
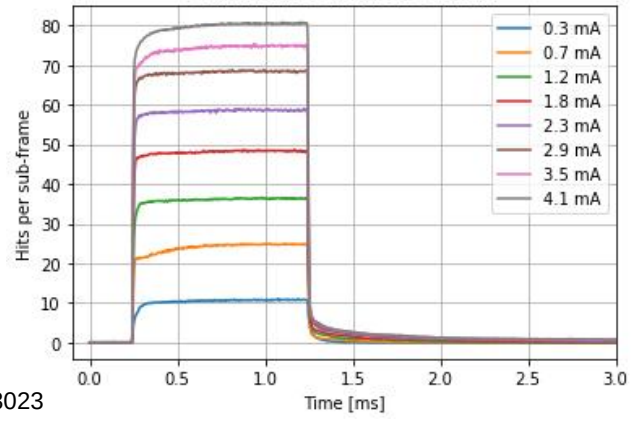
CURRENT STATUS OF THE PROJECT







Readout implementation discussed in: *J. Inst.* **16** P03023
*https://doi.org/*10.1088/1748-0221/16/03/P03023

Current work…

- Test sensors: 4 mm × 4 mm CdTe
  - Small pixel matrices of 100, 200 and 300 µm pitch
- Readout chip: TSMC CMOS 65nm
  - 2 stage 3-bit pipelined ADCs in the pixel
- Ongoing characterization
  - “Fighting” with CdTe sensors at high flux
  - Quest for better materials: CZT (?)

…and future plans:

- R&D phase (2019-2023)
- Final specifications defined at the end of the R&D
- Engineering phase planned from 2023