Active matrix back planes for the control of large area X-ray imagers

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Outlook

- Introduction / General considerations
- Amorphous silicon flat panel imaging technology
- Need for pixel electronics. Limitations of a-Si
- Alternative large areas technologies
  - Polysilicon
  - Nanowires
- Summary and conclusion

Solid state X-ray imagers

- c-Si based detectors
  - Linear arrays
    - Diodes
    - Microstrips
  - Two dimensional detectors
    - CCD: max surface ~ 8x10 cm^2 (eg., CCD595, Fairchild Imaging)
    - CMOS: max surface ~ 17x22 cm^2 (C7830-01, Hamamatsu)

⇩

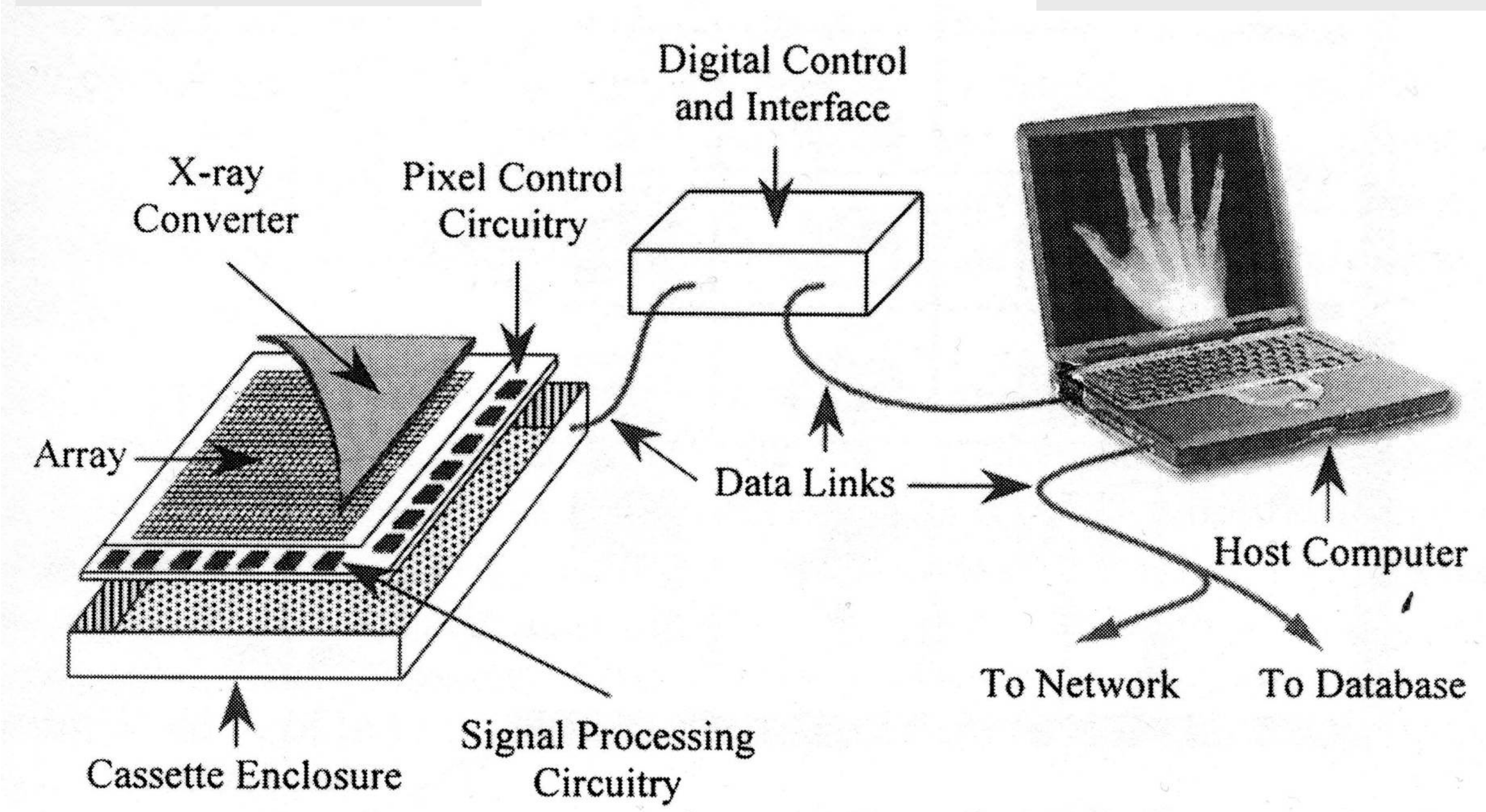
Wafer Scale Integration ⇒ Yield?

- a-Si:H based detectors

Active matrix flat panel X-ray imaging system

Immediate viewing
Digital processing
Image enhancement

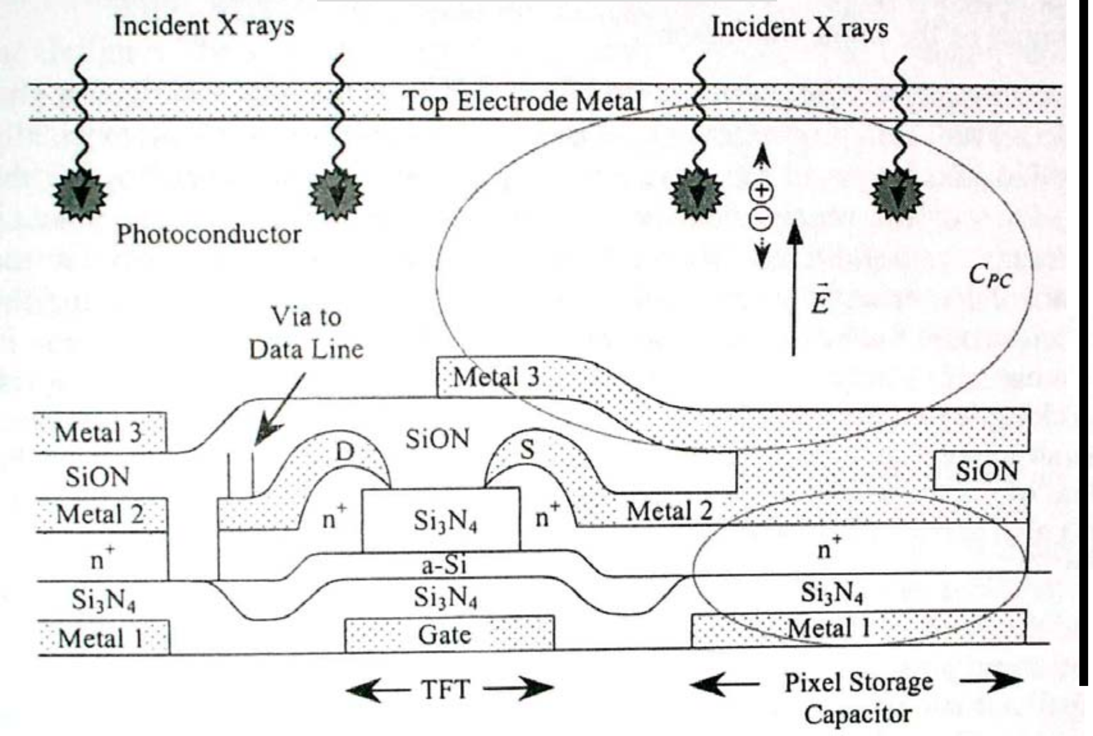
Electronic storage
Compactness
No chemical waste/photo



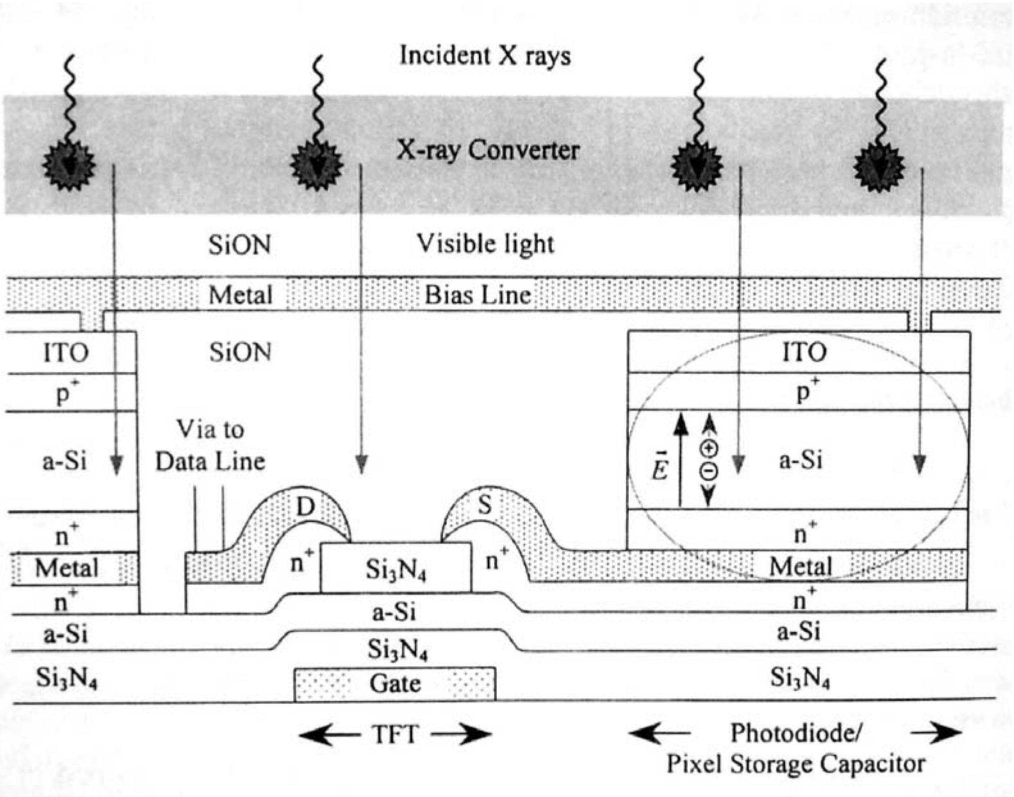
From L. Antonuk

The two detection schemes

Direct detection: photoconductor



X-rays ⇒ e-h pairs ⇒ q

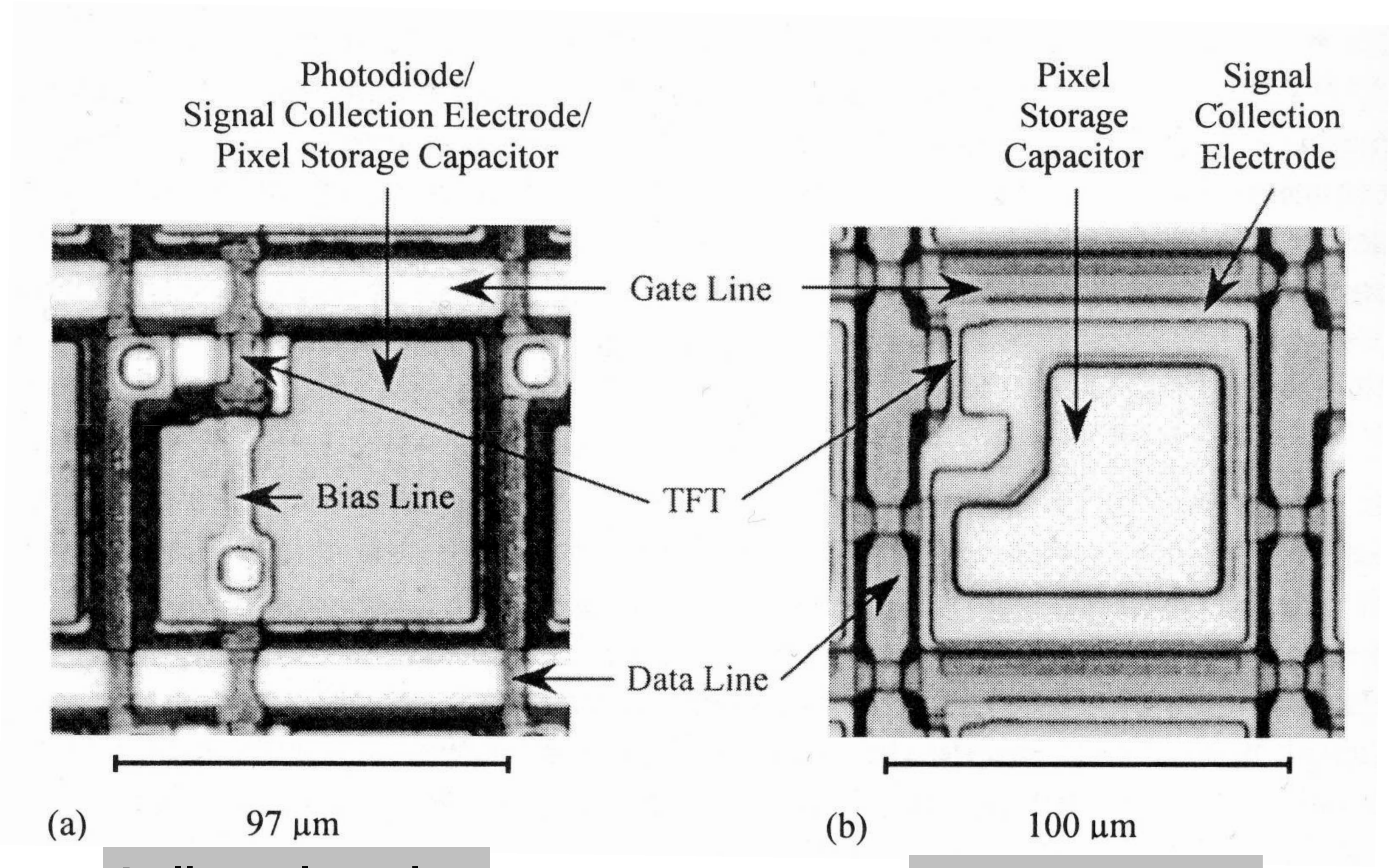


Indirect detection: p-i-n photodiode

X-rays ⇒ photons ⇒ e-h pairs ⇒ q

From L. Antonuk

Top view micrographs of individual pixels



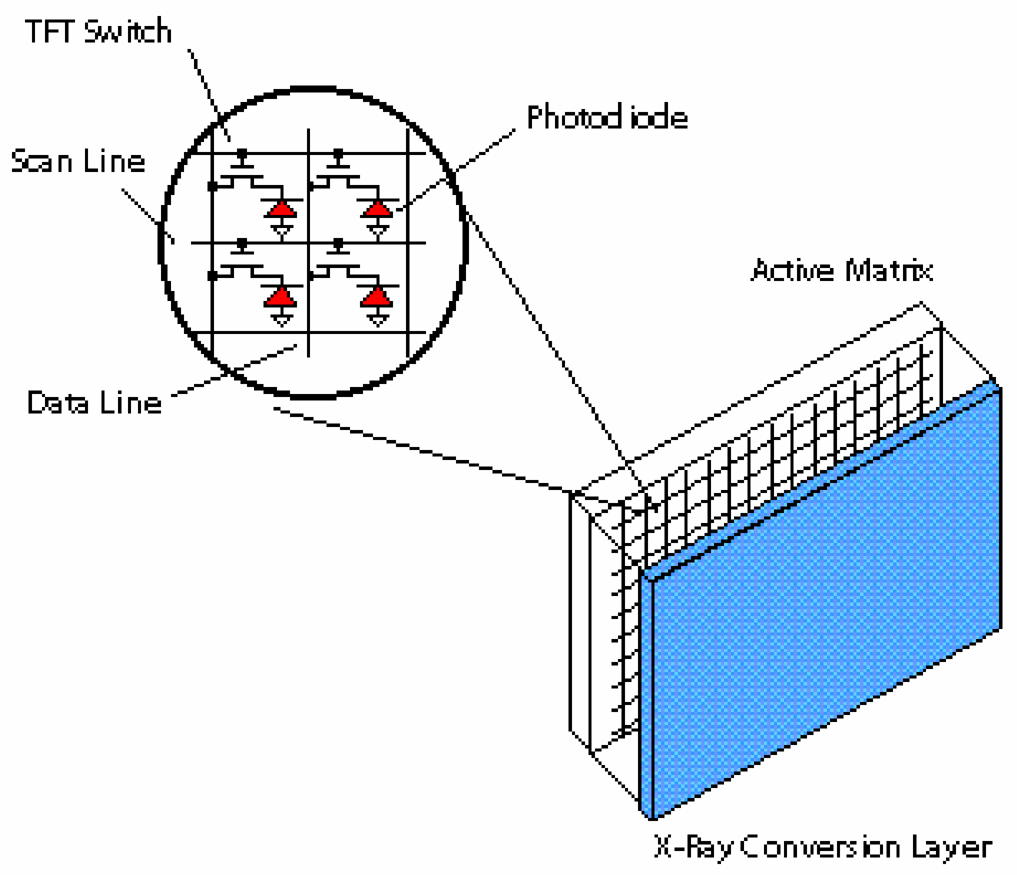
Indirect detection

Direct detection

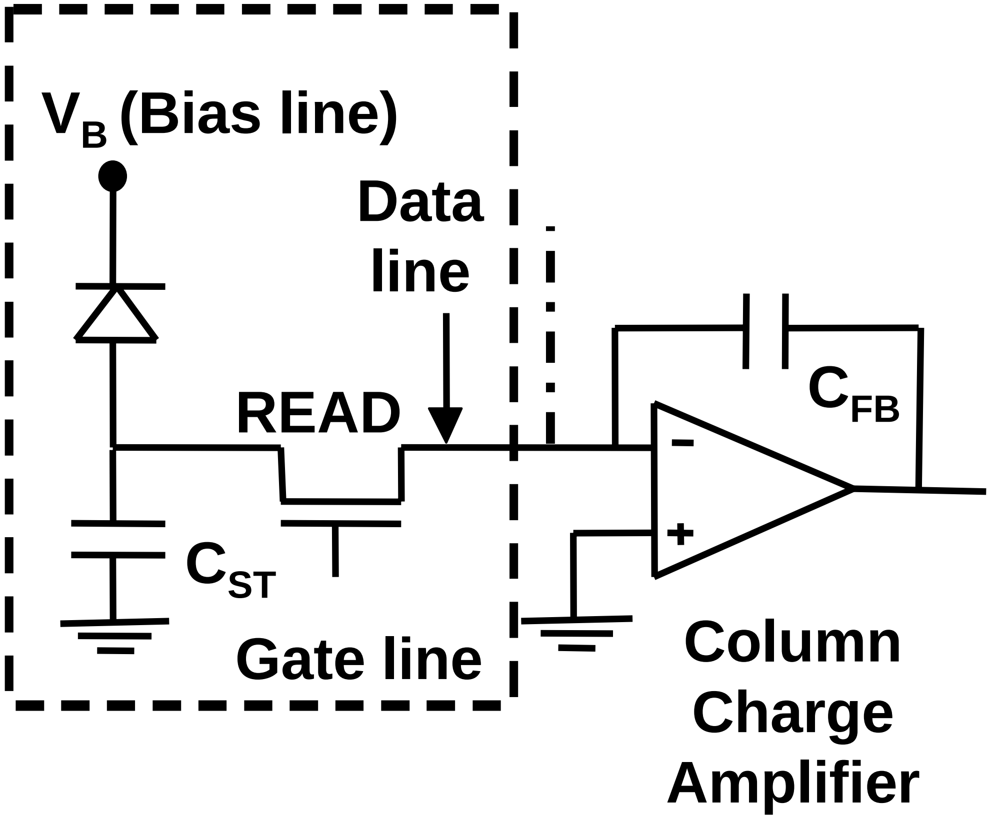
From L. Antonuk

General organisation of an active matrix detector

Imaging array



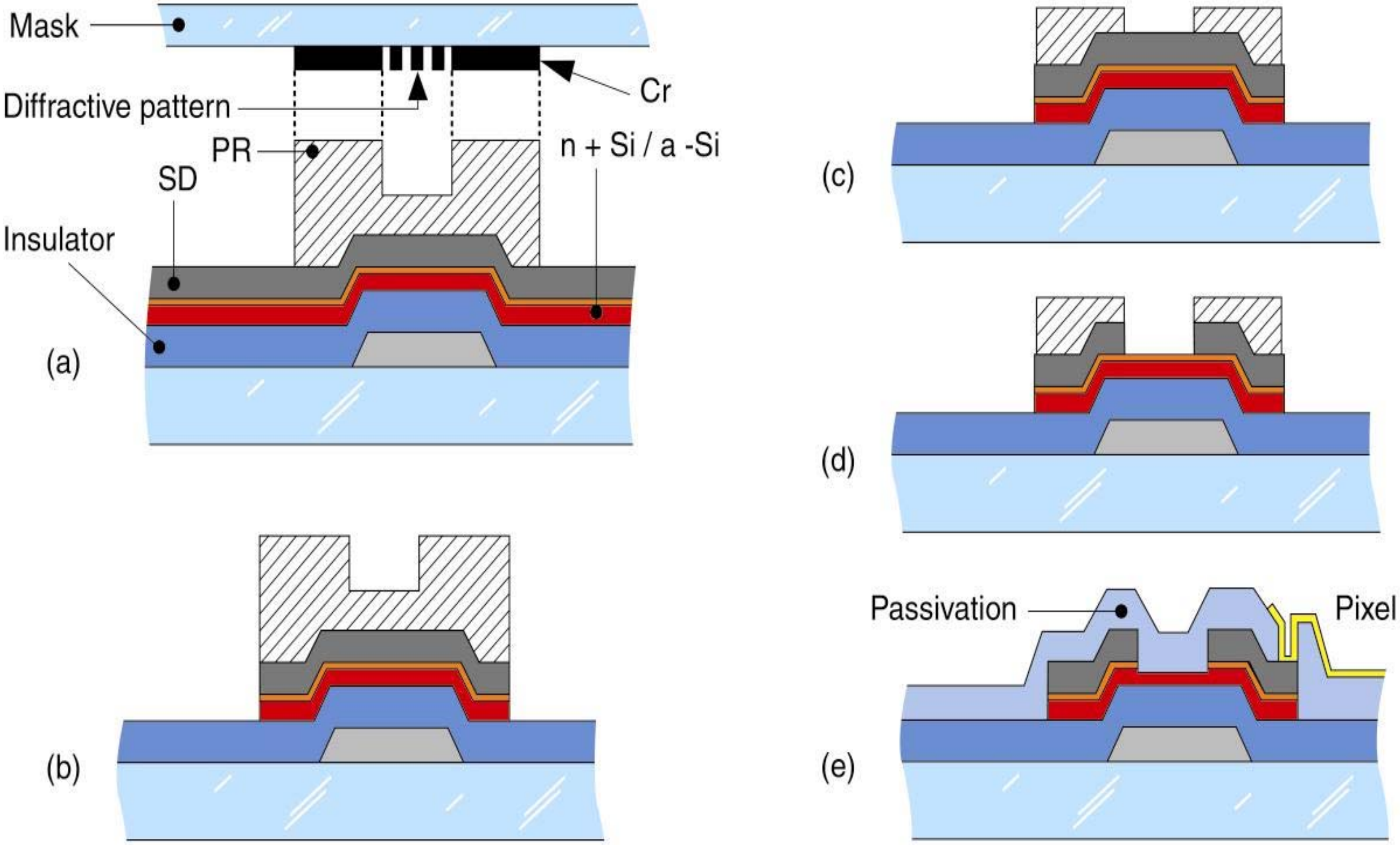
Pixell



Why a-Si:H?

- a-Si:H TFTs represent a very mature technology
  - – Used in AMLCDs (revenue of 48.5 G$ in 2004)
  - – 5 to 4 mask process for the active matrix
  - – Processed on 1.870x2.200 m^2 mother plates (gen. 7)
  - – Highly rad hard
- a-Si:H p-i-n photodiodes (indirect detection)
  - – Well matched with CsI:Tl (~ 550nm)
  - – Sub-µs response time ⇒ dynamic applications
  - – Low dark current ⇒ low exposure level

Advanced TFT process: down to 4 masks



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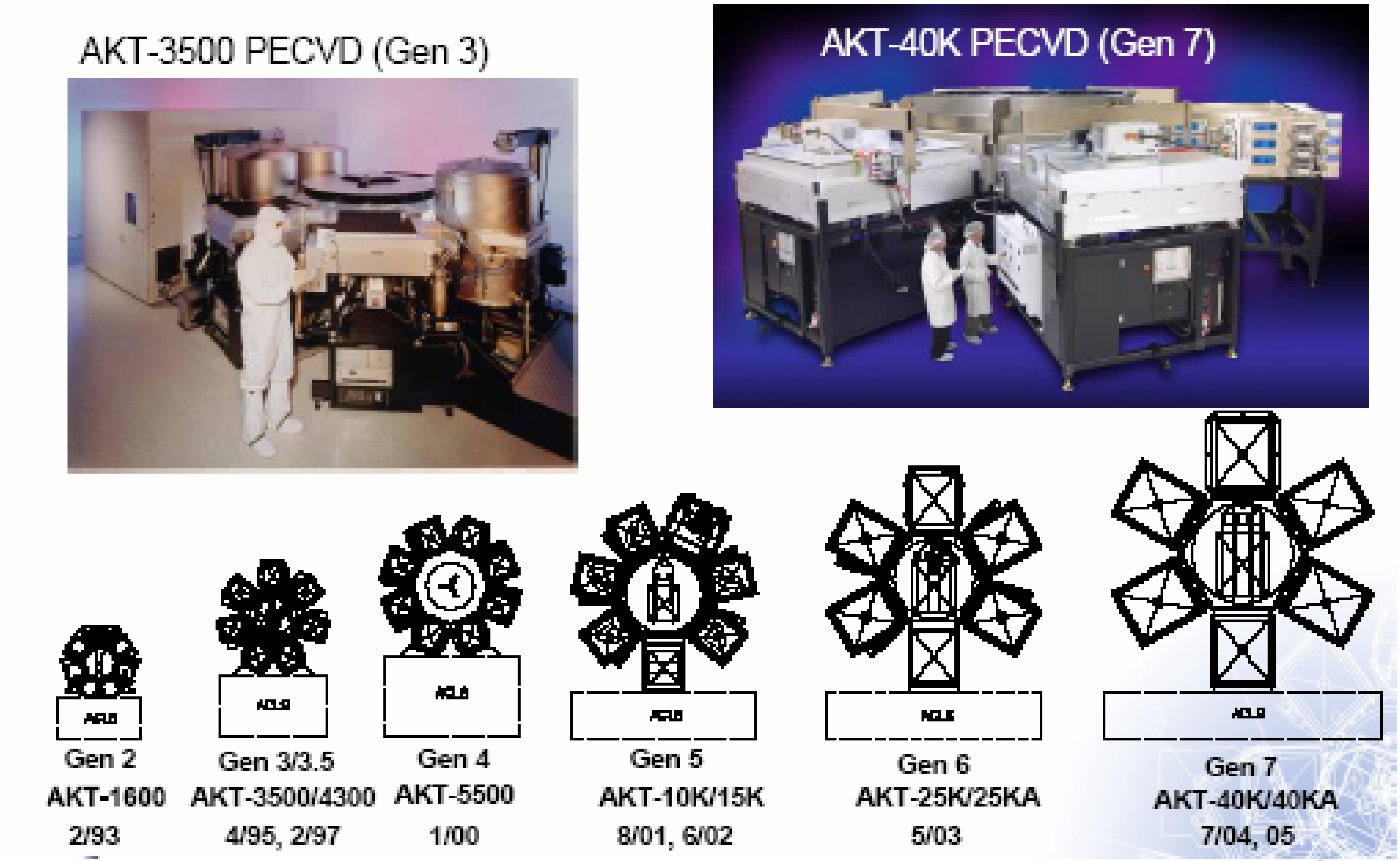
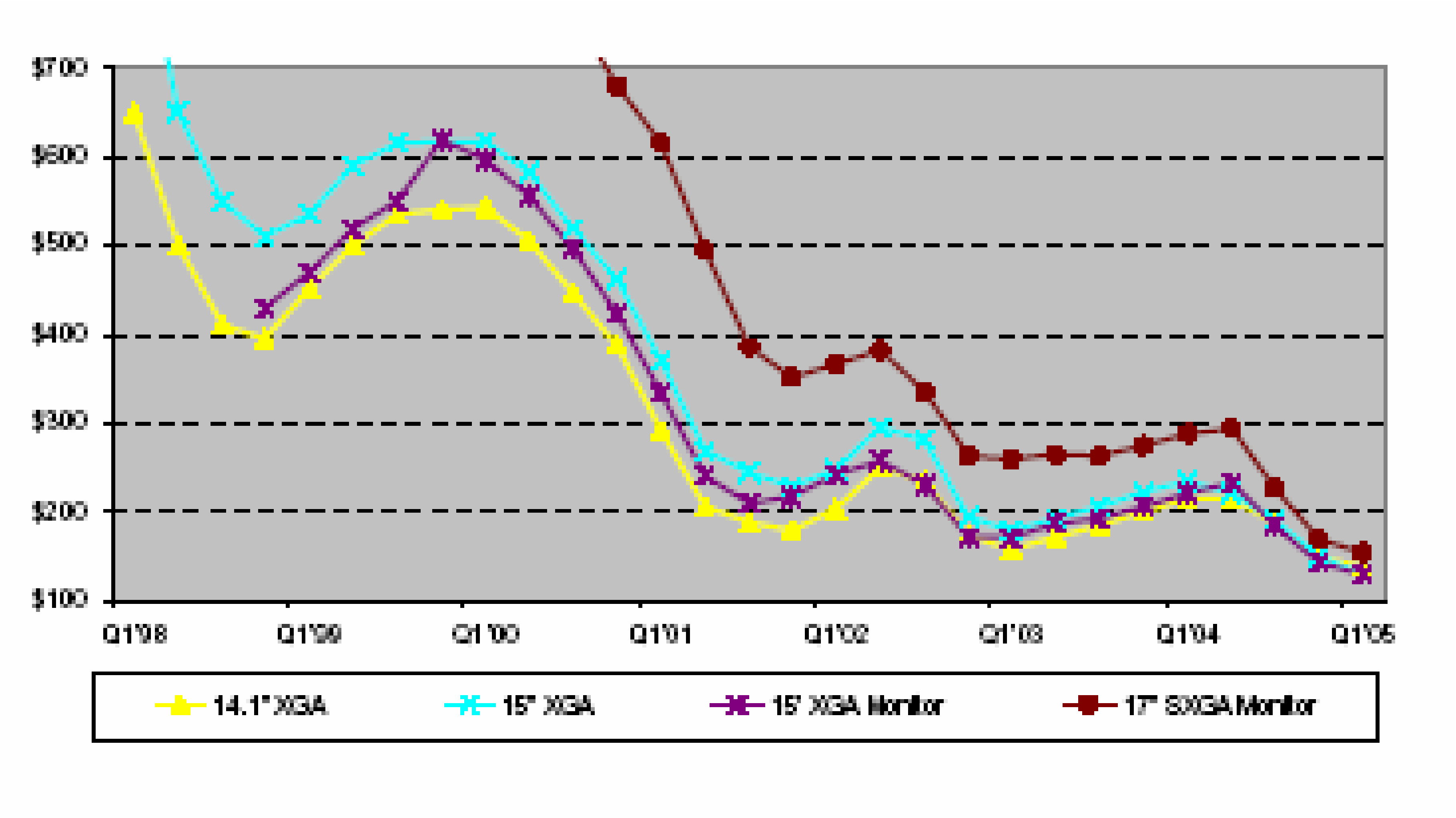
Evolution of PECVD systems (TFT stack deposition)



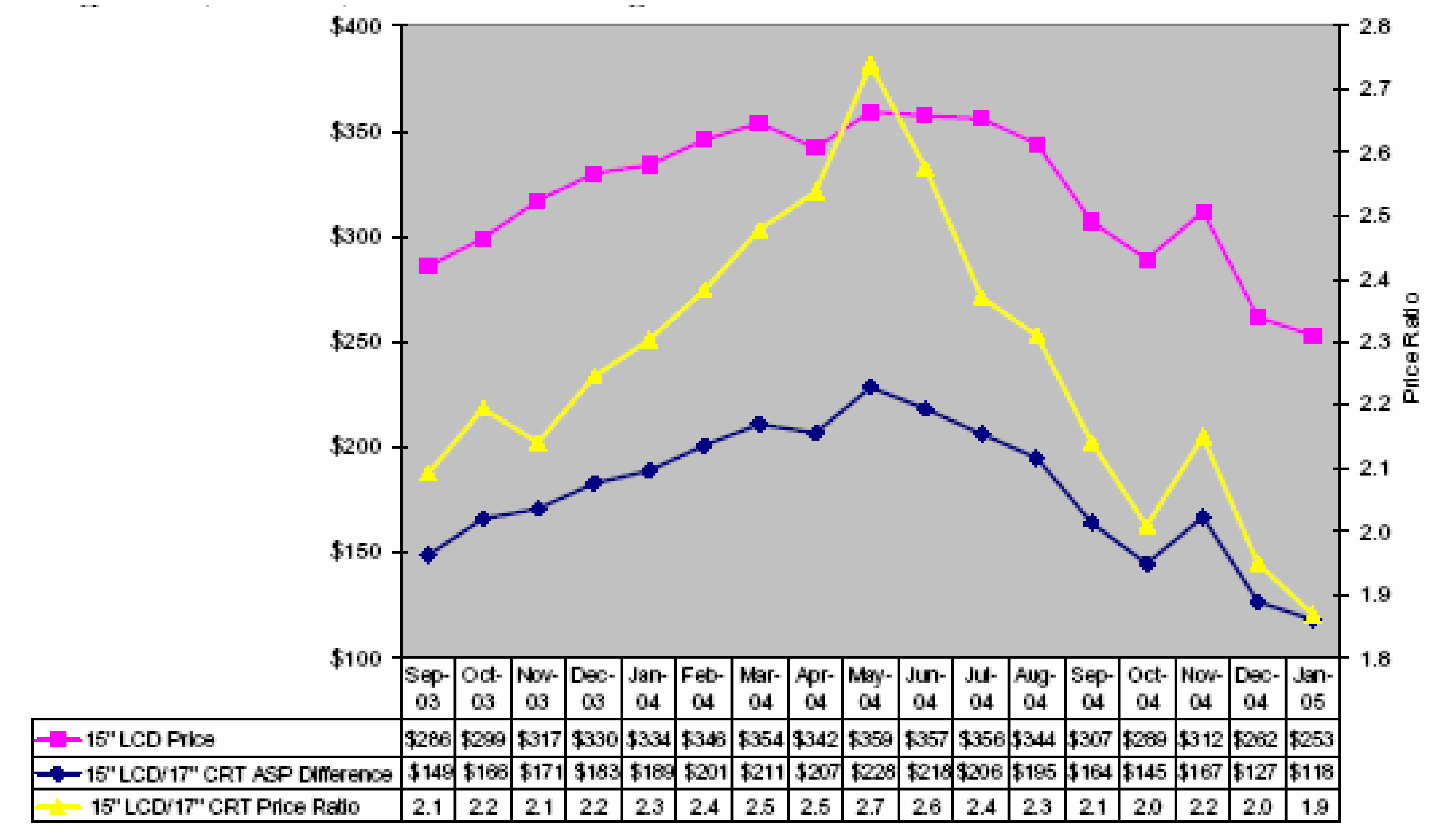
From AKT

Recent evolution of LCD panel prices



From Display Search

Street price of 15" TFT-LCD displays



	Sep-03	Oct-03	Nov-03	Dec-03	Jan-04	Feb-04	Mar-04	Apr-04	May-04	Jun-04	Jul-04	Aug-04	Sep-04	Oct-04	Nov-04	Dec-04	Jan-05
🟪 15" LCD Price	$286	$299	$317	$330	$334	$346	$354	$342	$359	$357	$356	$344	$307	$289	$312	$262	$253
◆ 15" LCD/17" CRT ASP Difference	$149	$166	$171	$183	$189	$201	$211	$207	$228	$218	$206	$195	$164	$145	$167	$127	$118
▲ 15" LCD/17" CRT Price Ratio	2.1	2.2	2.1	2.2	2.3	2.4	2.5	2.5	2.7	2.6	2.4	2.3	2.1	2.0	2.2	2.0	1.9

From Display Search

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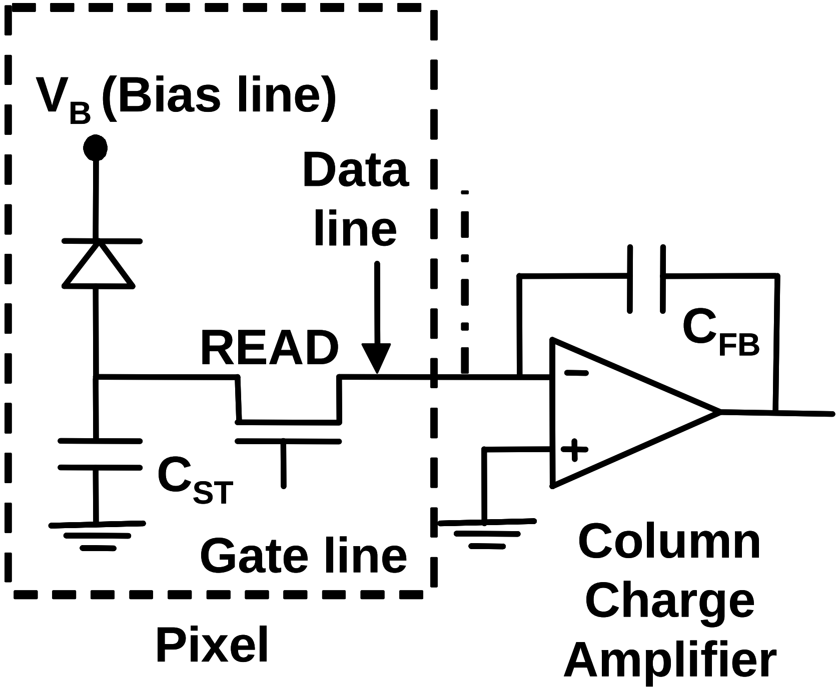
Some requirements for medical imaging

	Radiography	**Mammography**	**Fluoroscopy**
Imager size (cm)	35 x 43	18 x 24	25 x 25
Pixel area (µm^2)	150 x 150	50 x 50	250 x 250
Pixel count	1750 x 2150	3600 x 4800	1000 x 1000
Image readout time (s)	< 5	< 5	33 ms/frame
X-ray spectrum (kVp)	120	30	80
Exposure range (mR)	0.03 – 3	0.6 – 240	0.0001 – 0.01

Some limitations of active matrix imagers

Charge must be transferred through long data line:
⇒ Column capacitance limits noise performance of charge amplifiers
⇒ Coupling introduces pick-up noise
Thermal noise in the pixel TFT:
⇒ $(kTC_{ST})^{1/2}$ noise ~ 500 e-rms

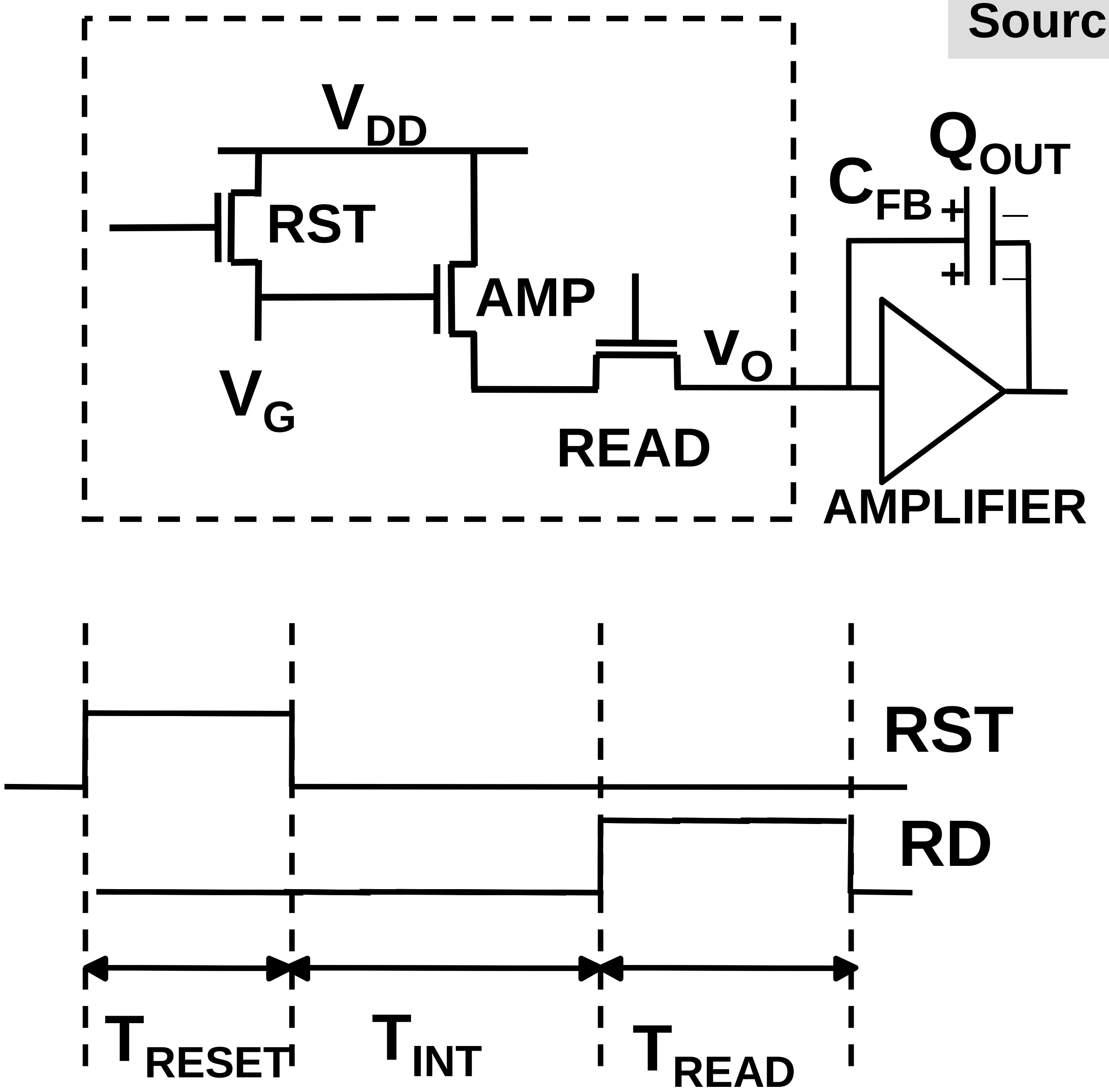


Challenge for fluoroscopy
(~ 1000 electrons for a-Se photocond)

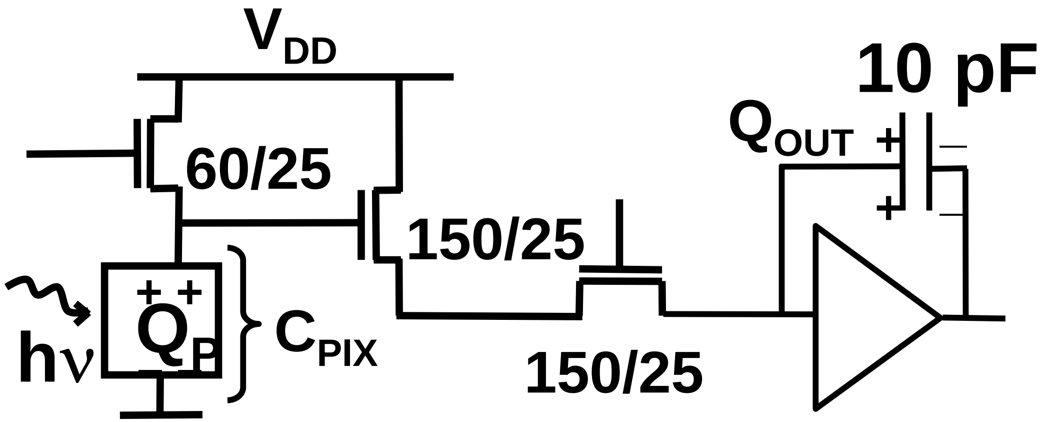
Increase SNR:
- High pixel fill factor
- Pixel amplification

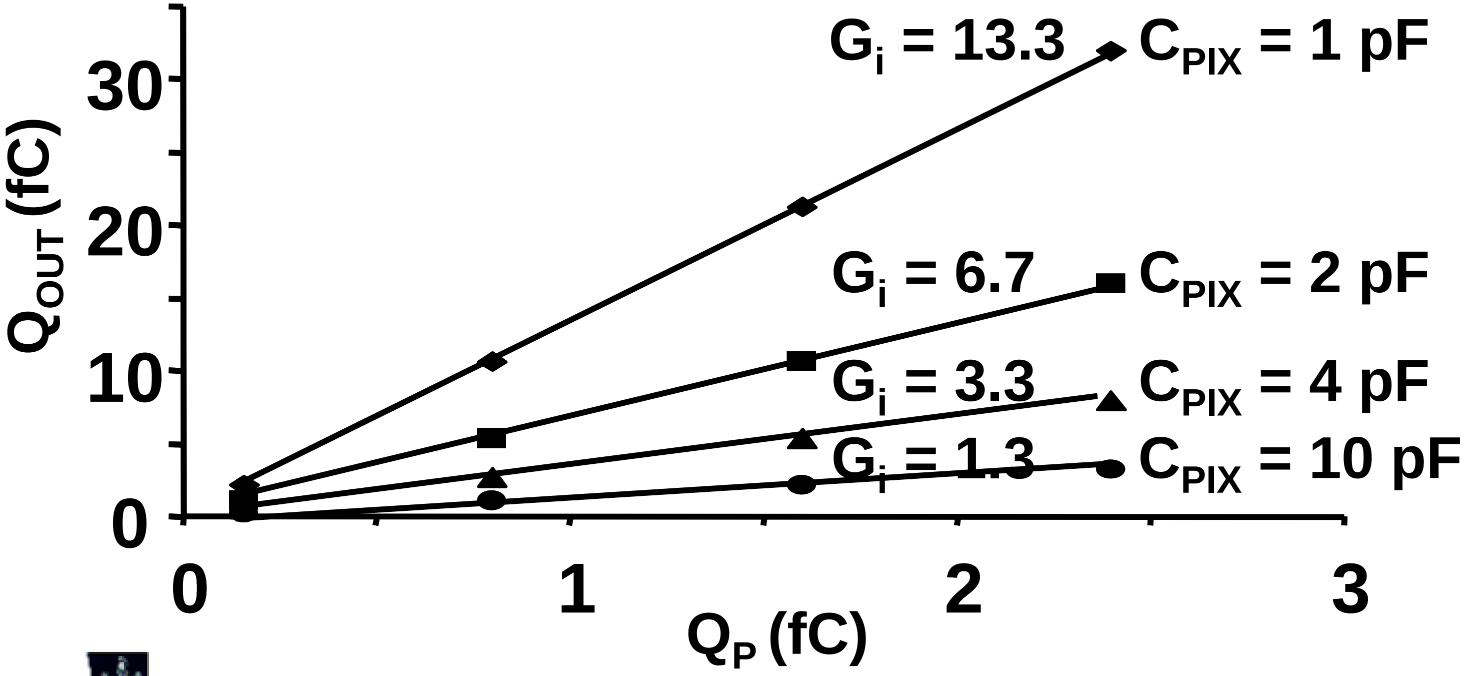
Pixel amplification

Source follower circuit



Charge gain for pixel amplification (a-Si:H TFTs)





OK for fluoroscopy but signal saturation for radiography!!

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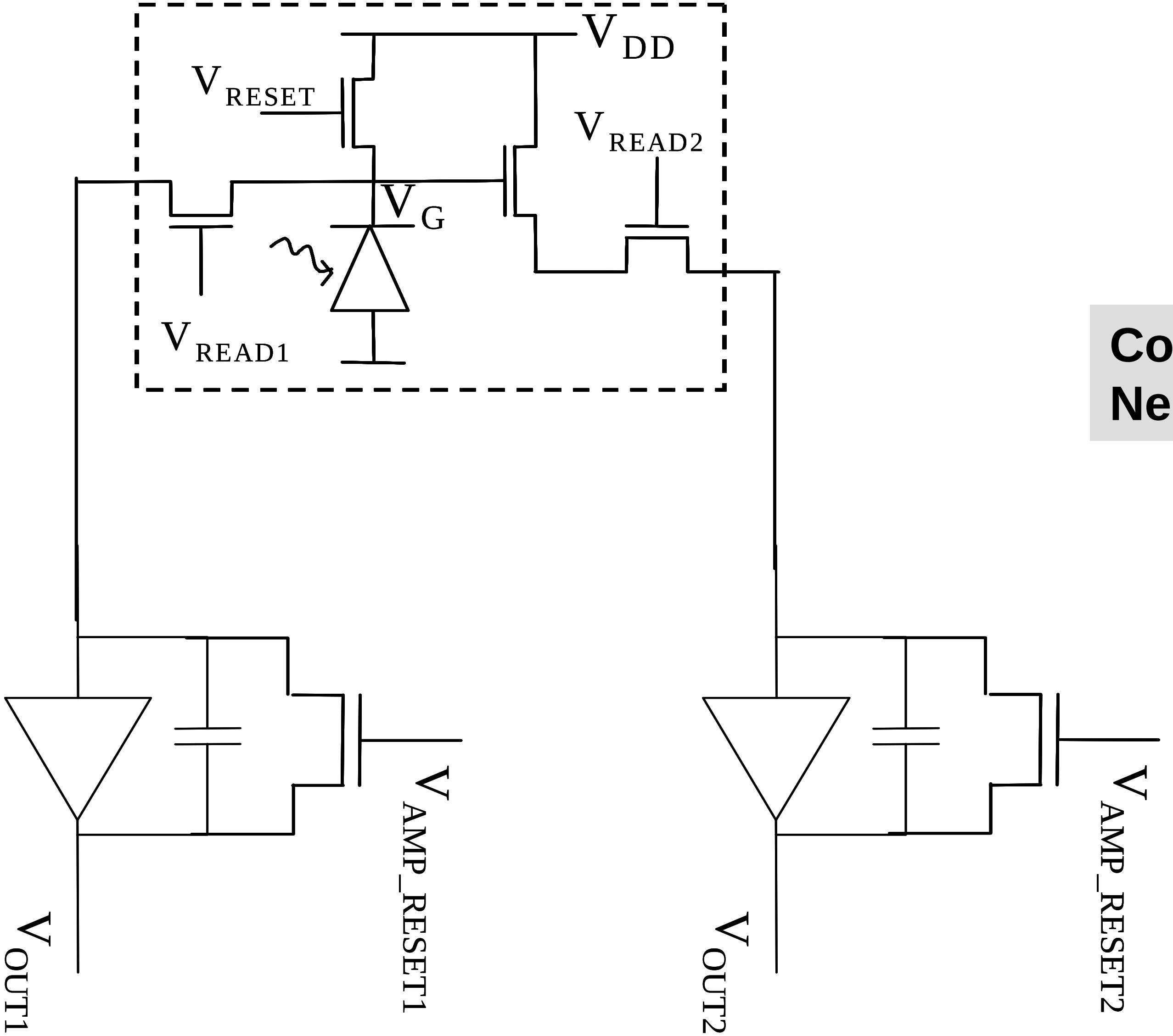
K.S. Karim, ITC '05

High dynamic range pixels



Conclusion:
Need for pixel circuitry!!

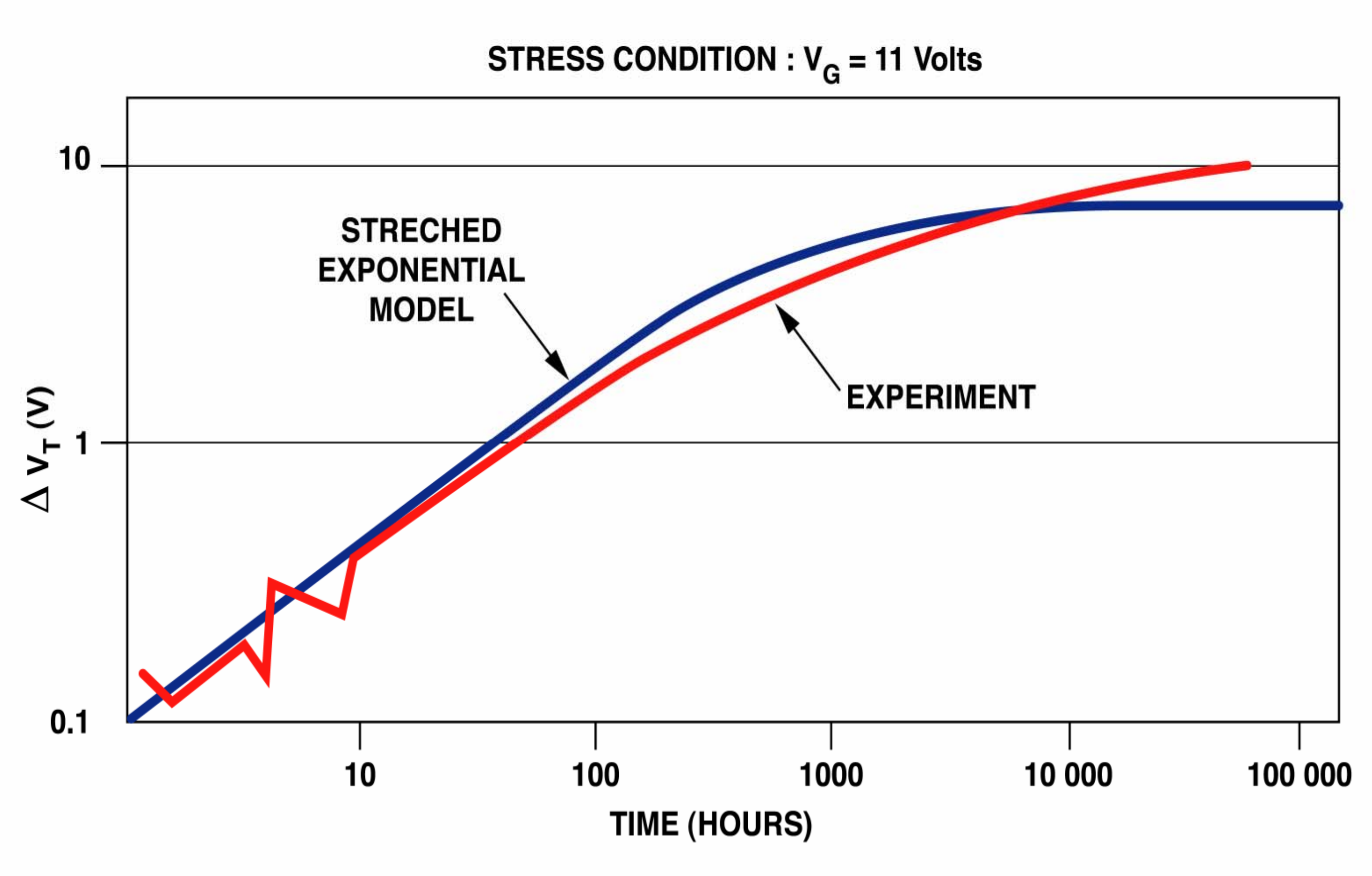
a-Si drawbacks for circuits

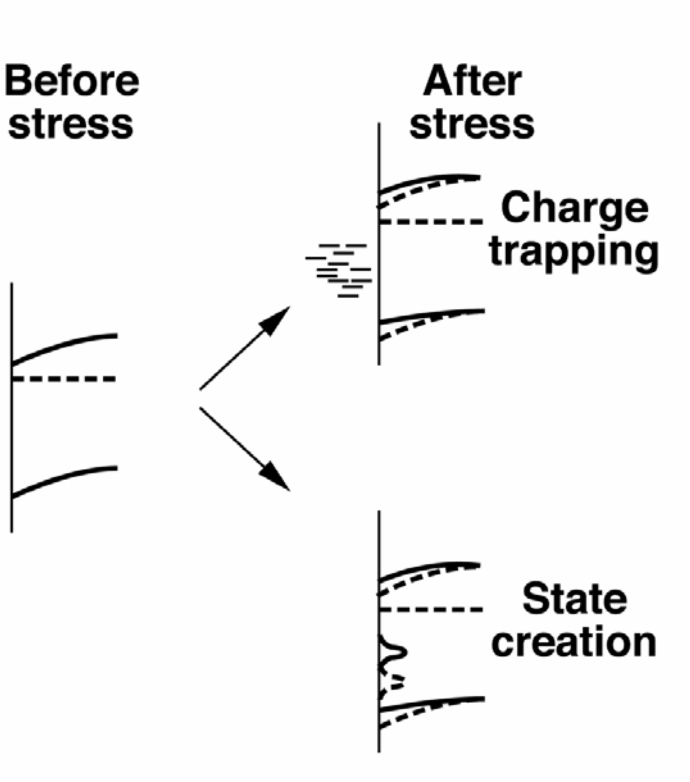
Metastability

Poor transport properties

- ⇒ large TFTs
- ⇒ parasitic effects
- ⇒ Small fill factor. Need for stacked sensor structure

a-Si:H drawbacks for circuits





OK if low duty cycle

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D. Pribat

CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

a-Si drawbacks for circuits

Metastability

Poor transport properties

- ⇒ Large TFTs
- ⇒ Parasitic effects ⇒ Noise increase
- ⇒ Small fill factor. Need for stacked sensor structure

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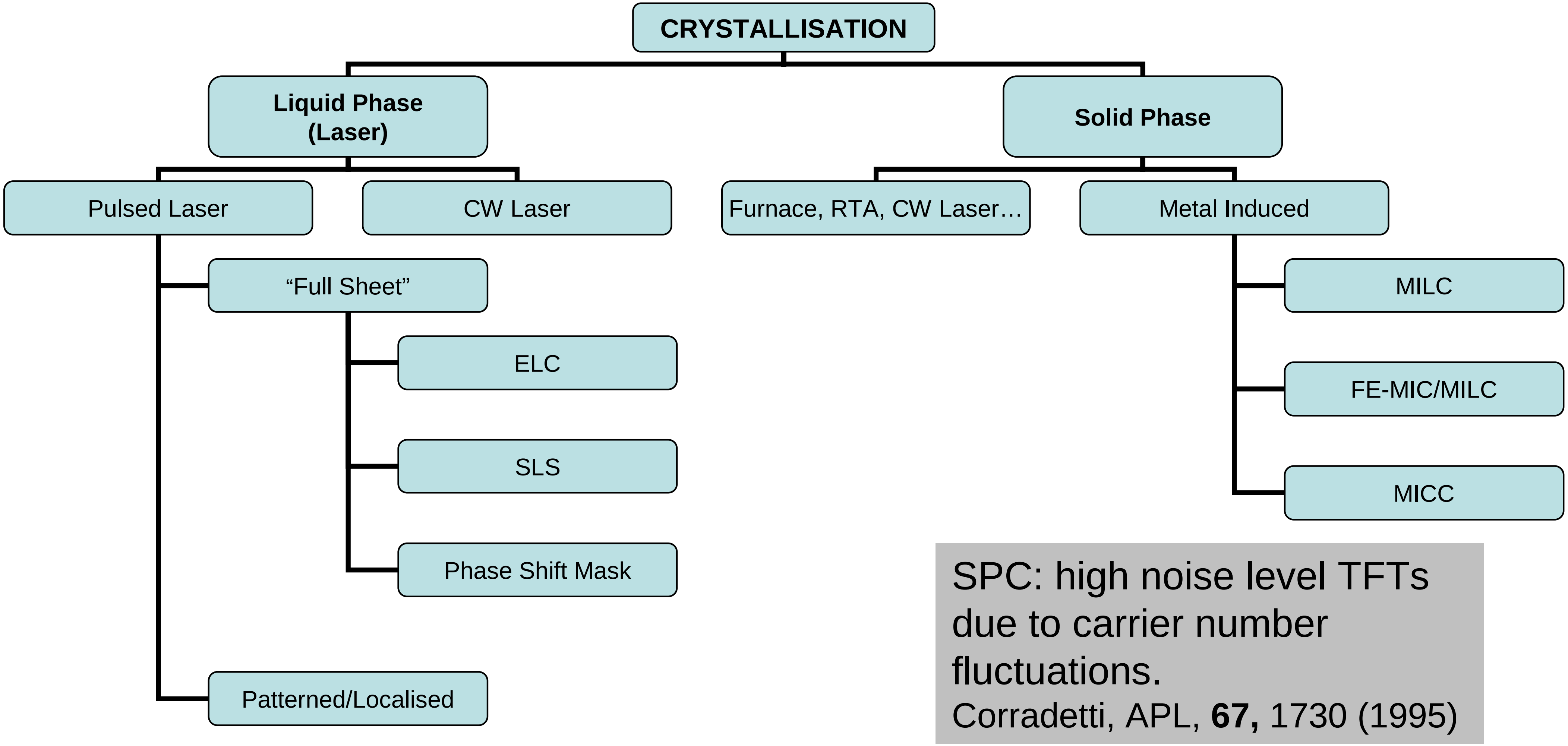
Alternative technologies

→ Poly-Si

→ Si Nanowires

The various crystallisation processes for Si on glass



CRYSTALLISATION

- **Liquid Phase (Laser)**
  - Pulsed Laser
    - "Full Sheet"
      - ELC
      - SLS
      - Phase Shift Mask
    - Patterned/Localised
  - CW Laser
- **Solid Phase**
  - Furnace, RTA, CW Laser…
  - Metal Induced
    - MILC
    - FE-MIC/MILC
    - MICC

SPC: high noise level TFTs due to carrier number fluctuations.
Corradetti, APL, **67,** 1730 (1995)

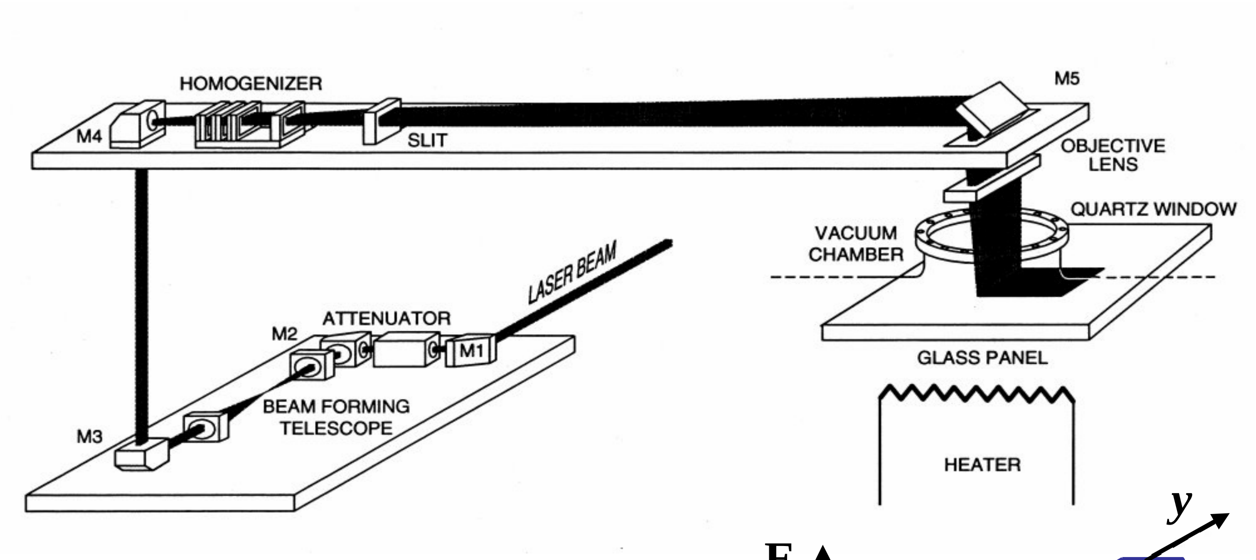
Crystallisation of a-Si: pulsed laser system with line beam optics

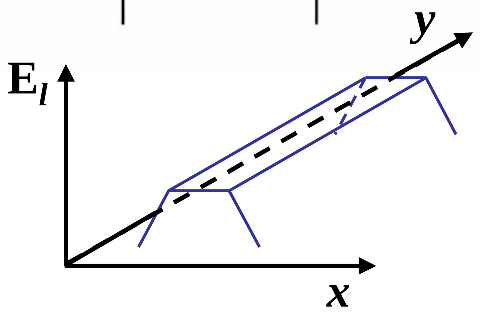
$L = (D\tau)^{1/2}$

$D = \kappa/\rho C_p$

L ~100 nm in SiO_2, for τ ~25 ns

XeCl, 308 nm, 50Hz

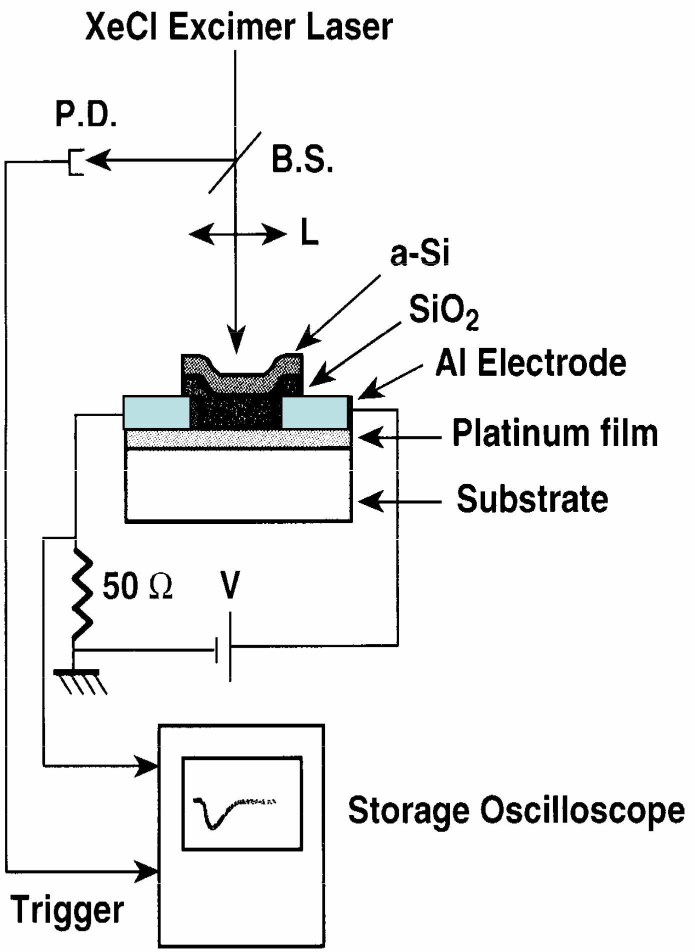


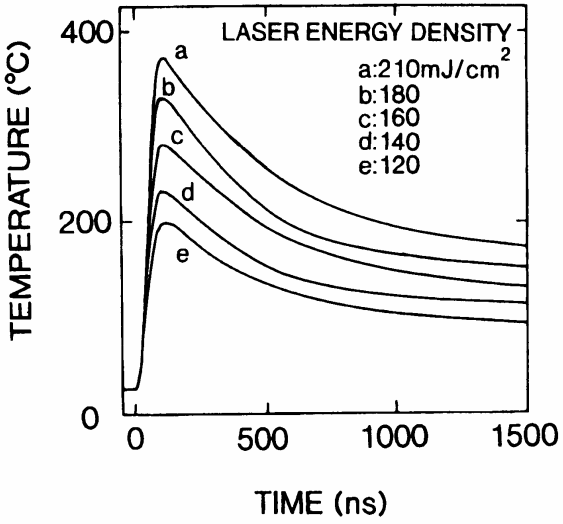


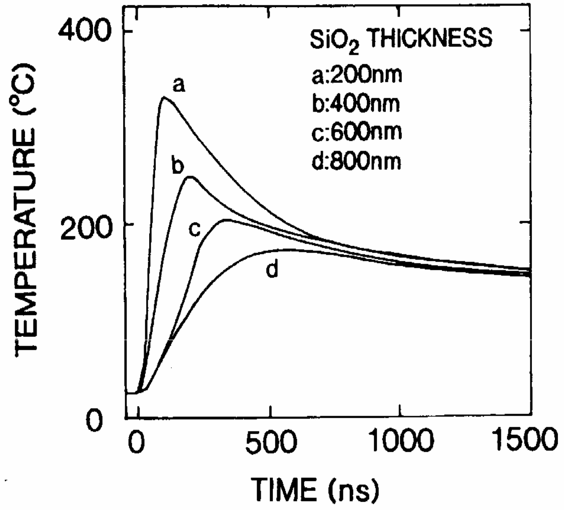
Top-hat energy profile

Largest line beam (Microlas):
350 mm X 250 µm

Why pulsed laser?





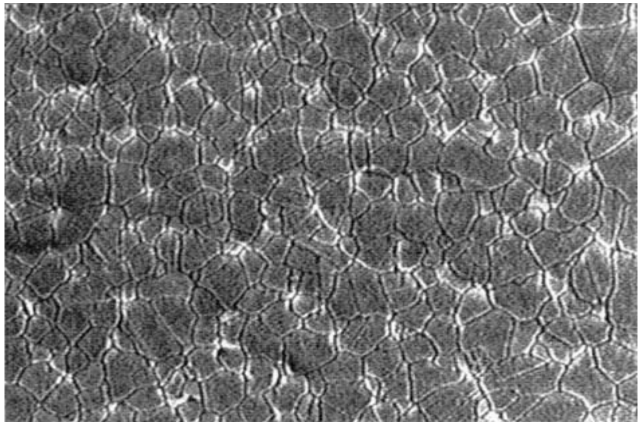


Poly-Si pros and cons

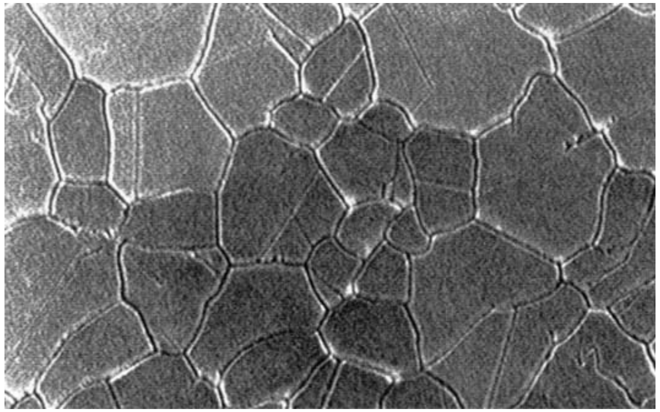
- High mobility TFTs (μ_n ~ 350 cm^2/Vs. μ_p ~ 150 cm^2/Vs)
- Low noise level TFTs (Carluccio, APL 71, 578,1997)
- Low Vth
- Self-aligned TFTs

- BUT:
  - Complex, small process window for high quality TFTs
  - Vth dispersion (grain size uniformity)
  - Surface roughness (reliability)
  - Non stabilised technology
  - Niche applications in displays so far, although studied for 2 decades

Grain size as a function of laser energy density (1)

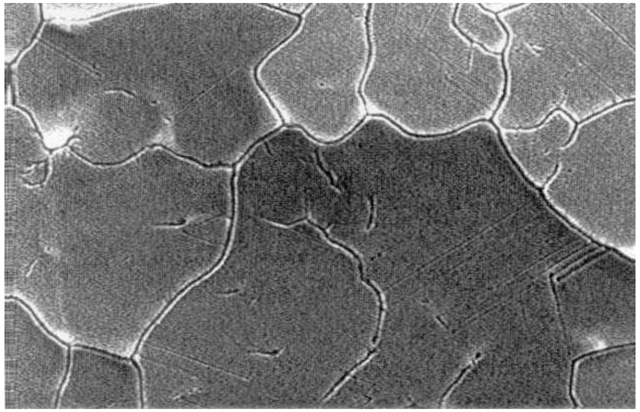


E = 360 mJ/cm^2

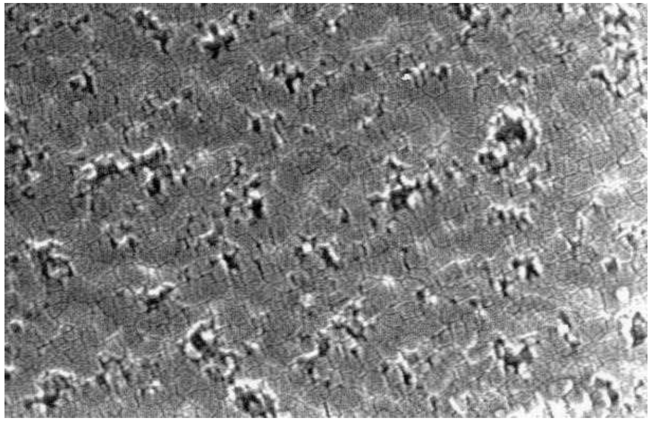


E = 400 mJ/cm^2

500 nm

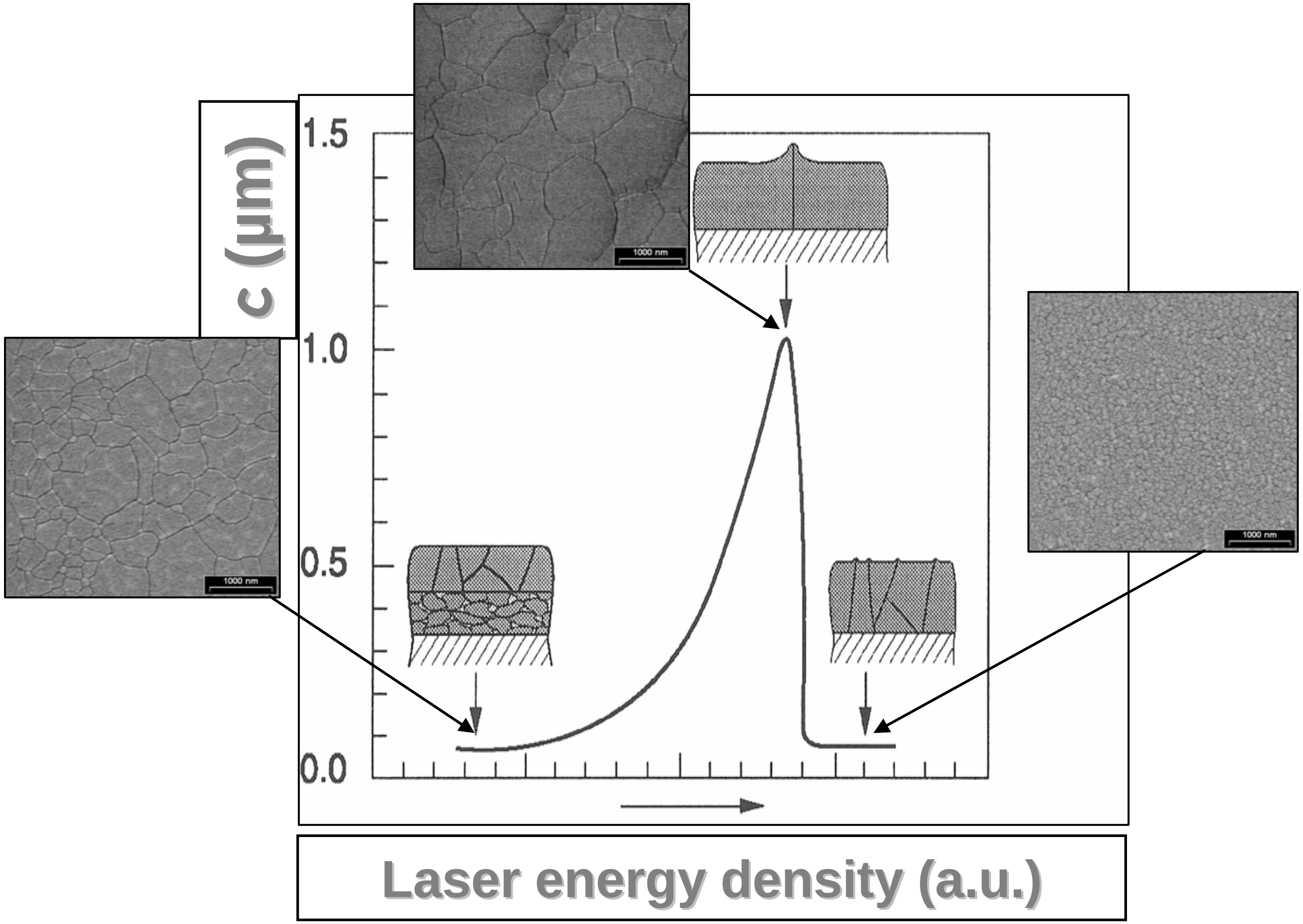


E = 430 mJ/cm^2



E = 470 mJ/cm^2

Grain size as a function of laser energy density (2)



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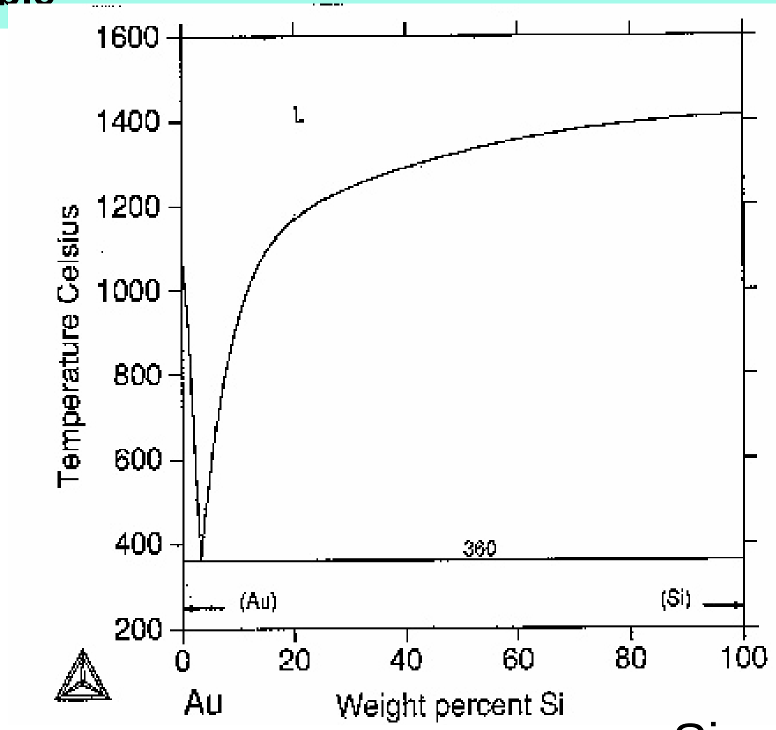
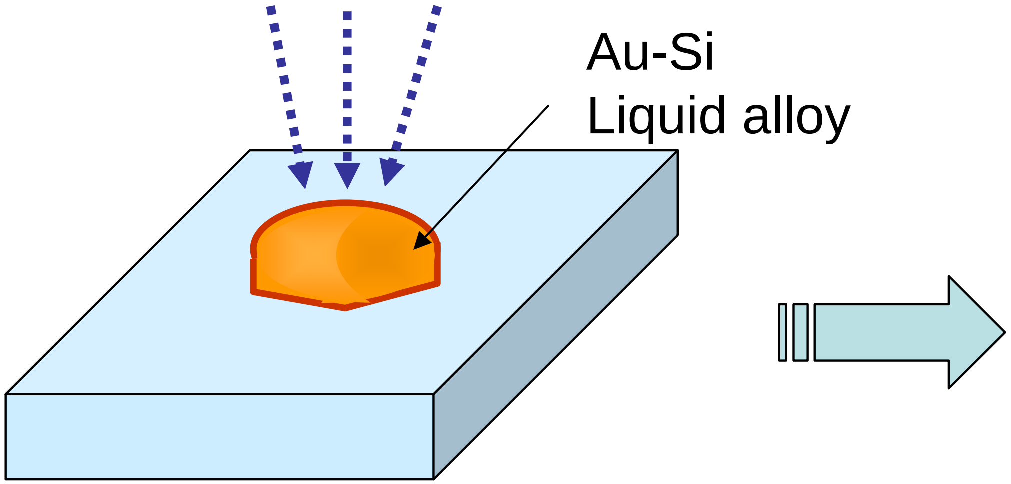
Semiconductor nanowires

- Si nanowires studied for CMOS replacement.
- However:
  - They can be grown at low to moderate T,
  - No need for refractory substrate,
  - No need for monocrystalline substrate.

→ Interest for displays and imagers!!

Principle of the VLS Growth method: Synthesis of NWs



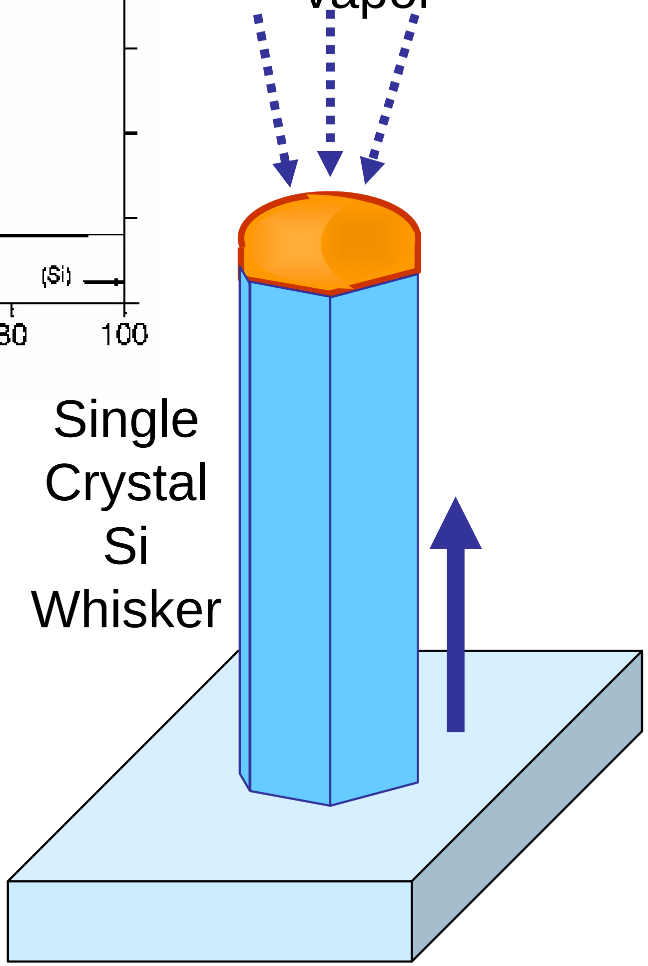


Vapor:
SiH$_4$,
or SiH$_4$ + PH$_3$ or B$_2$H$_6$

Au-Si
Liquid alloy

substrate

T ~ 400°C



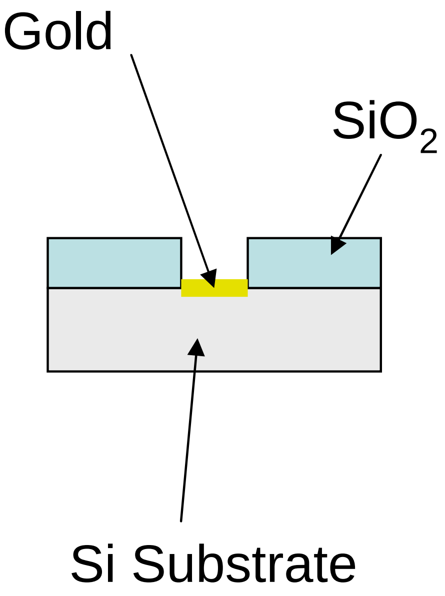
vapor

Single
Crystal
Si
Whisker

VLS growth of Si µ-wire arrays

T ~ 550°C

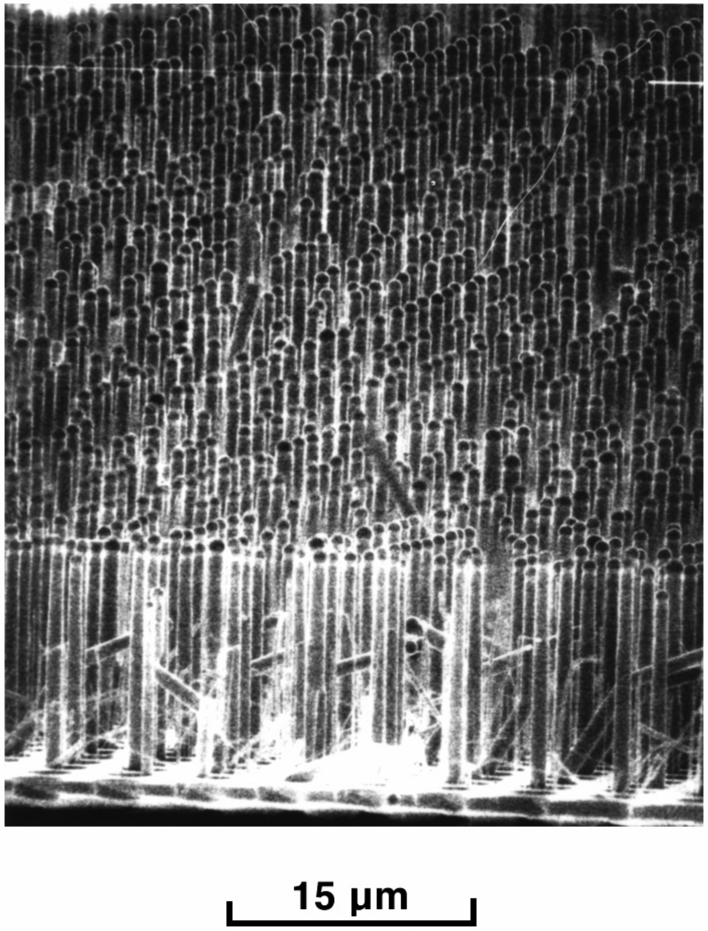
$SiH_4 + H_2$

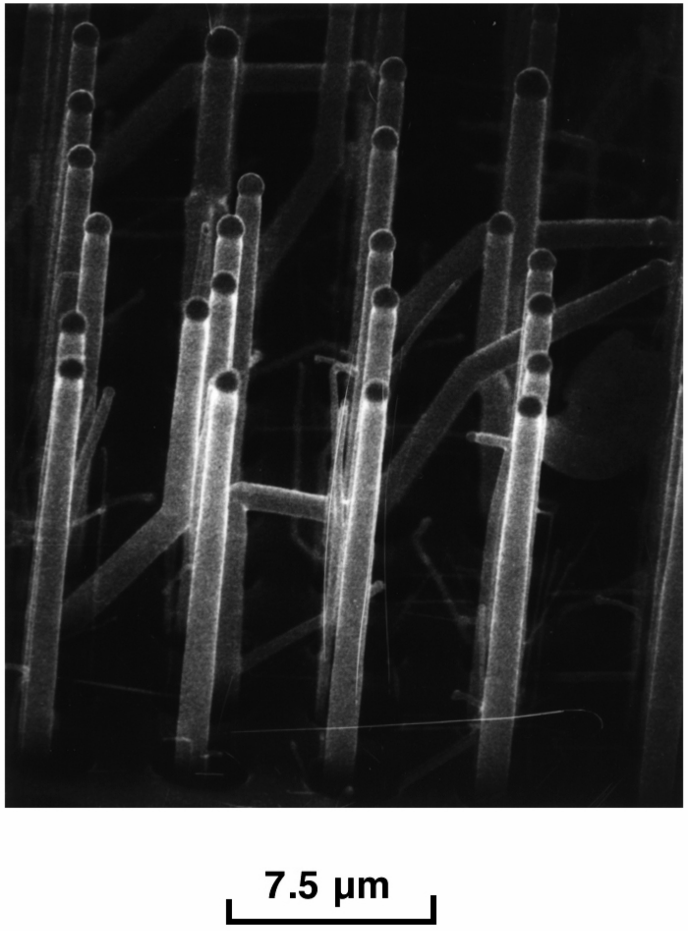


Gold

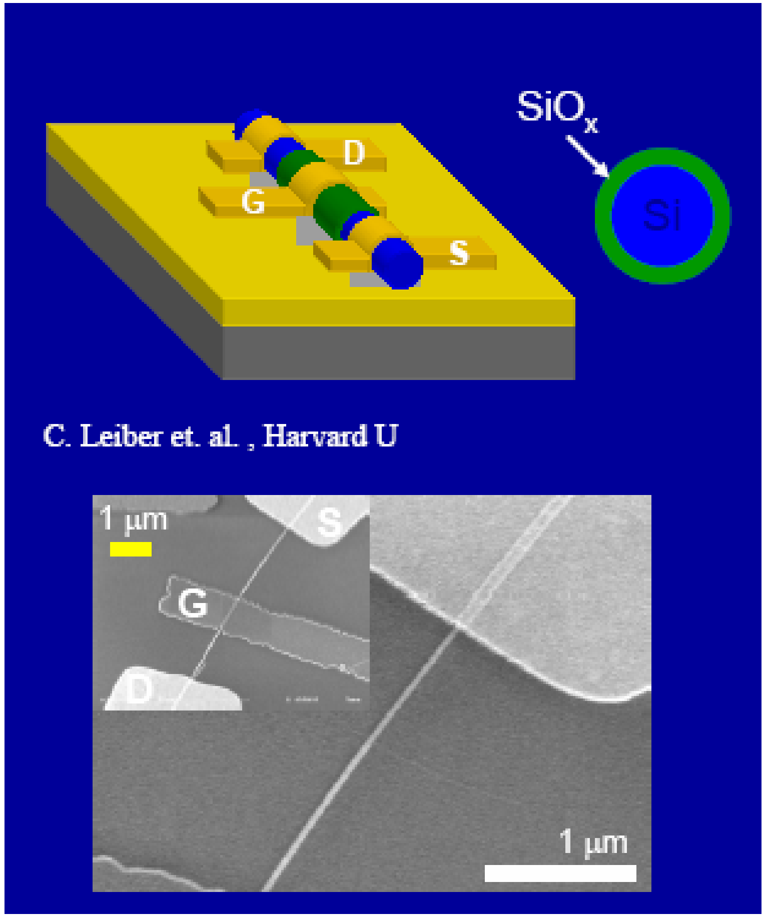
SiO_2

Si Substrate

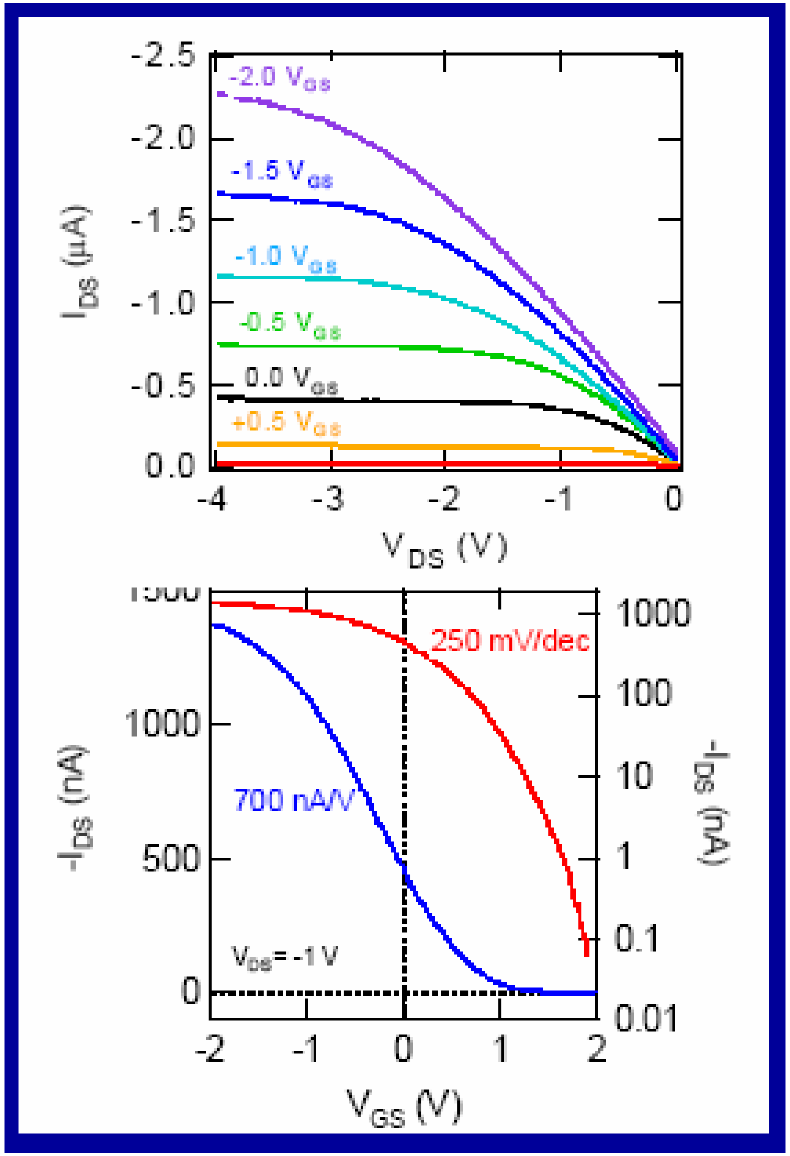




Si NanoWire FET



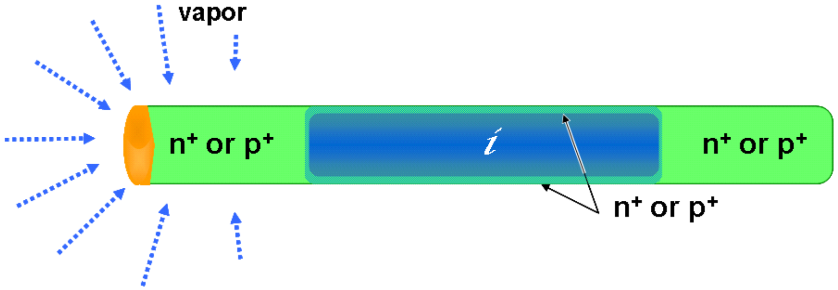
C. Leiber et. al. , Harvard U



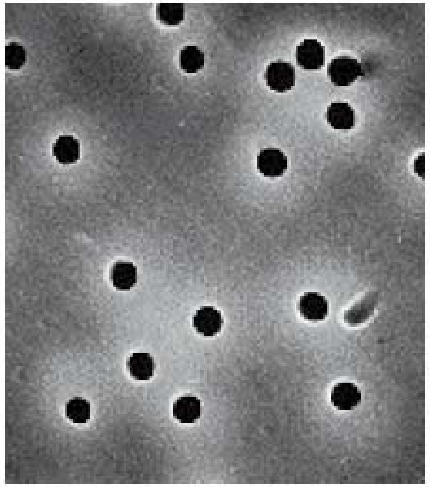
μ ~ 1350 cm^2/Vs
Lieber, *Nano Lett.*, 2003

Challenges with nanowires

- How to manipulate NWs?
- How to organise them?
- Controlled doping

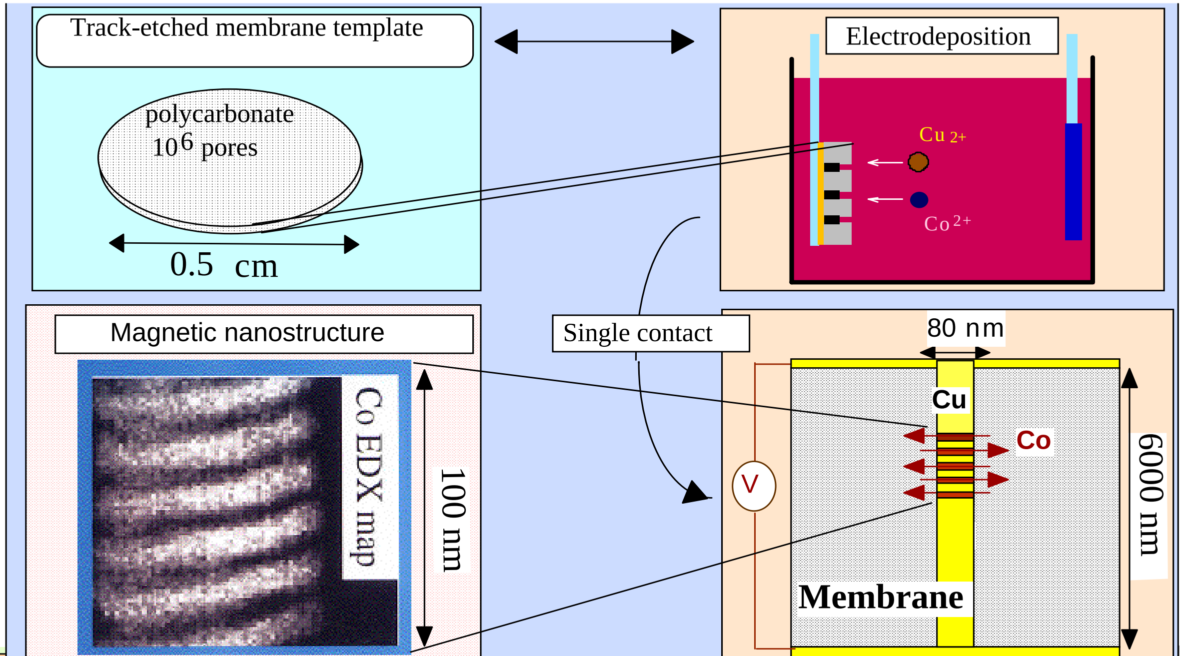


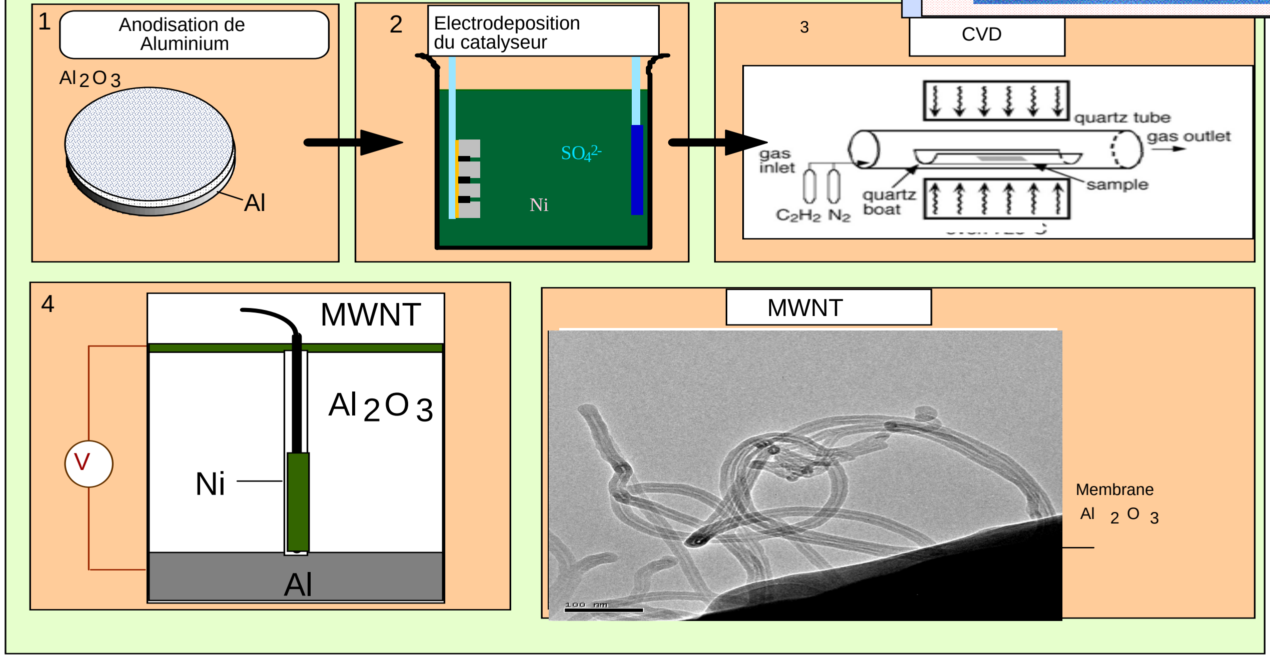
Template synthesis and structuring of nanomaterials (NWs and CNTs)

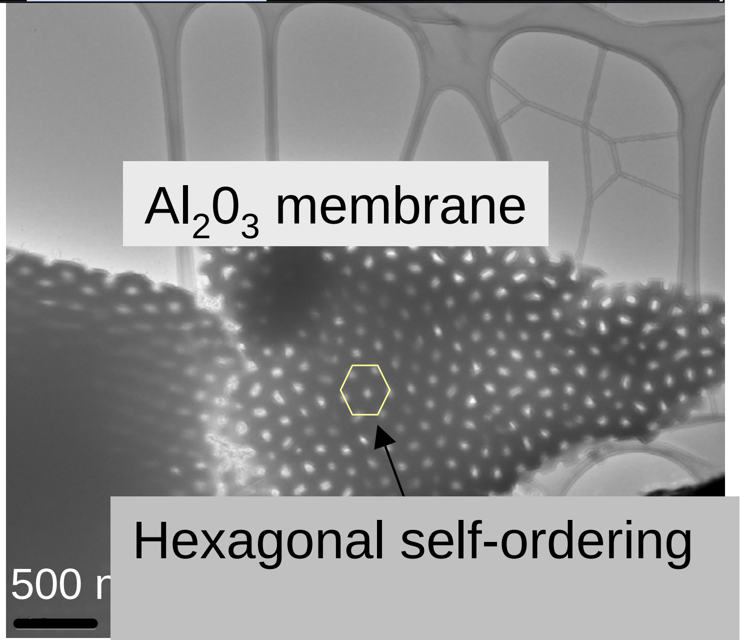


Polycarbonate membrane (random order)

Wade & Wegrowe,
Europ. Phys. J. Appl. Phys. 2005



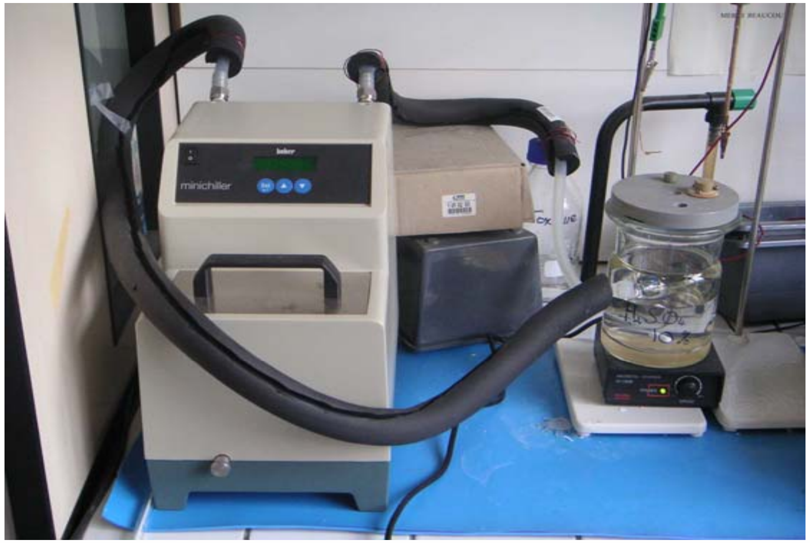


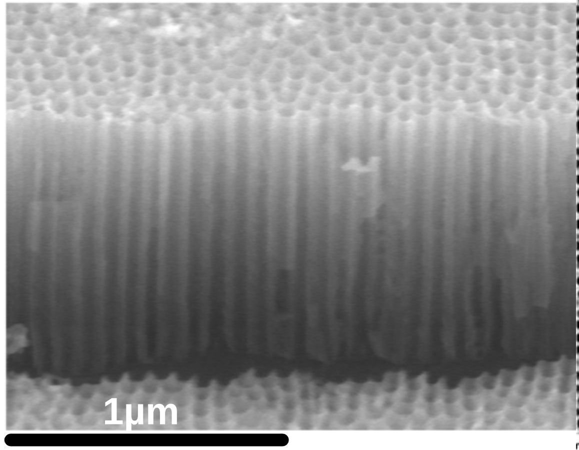


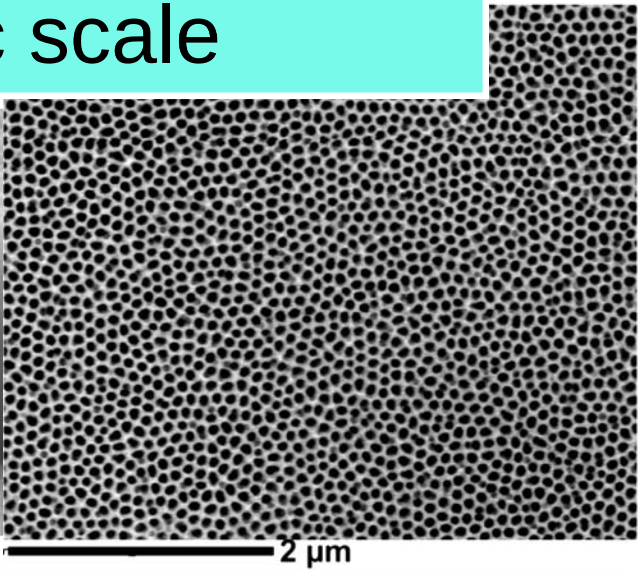
Al_2O_3 membrane

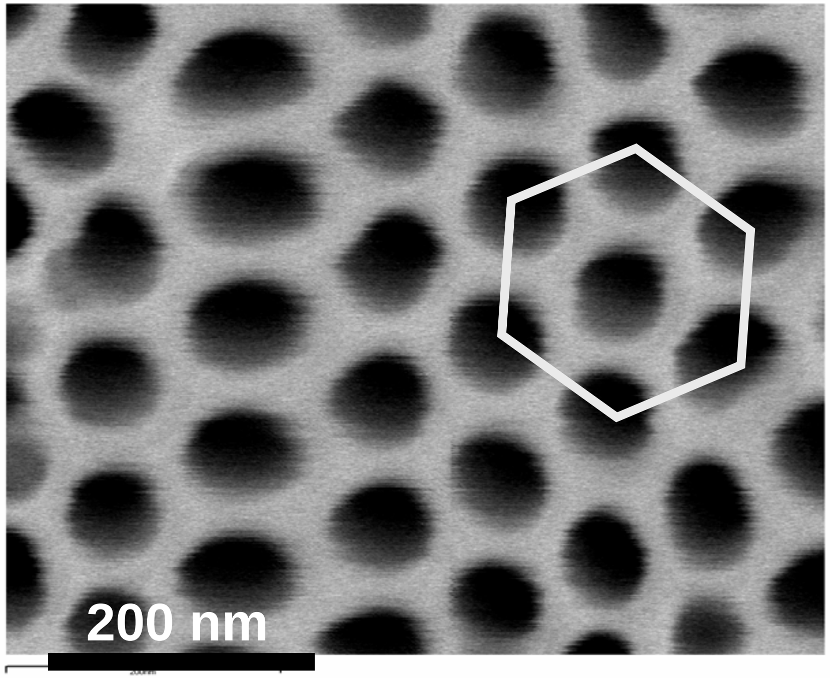
Hexagonal self-ordering

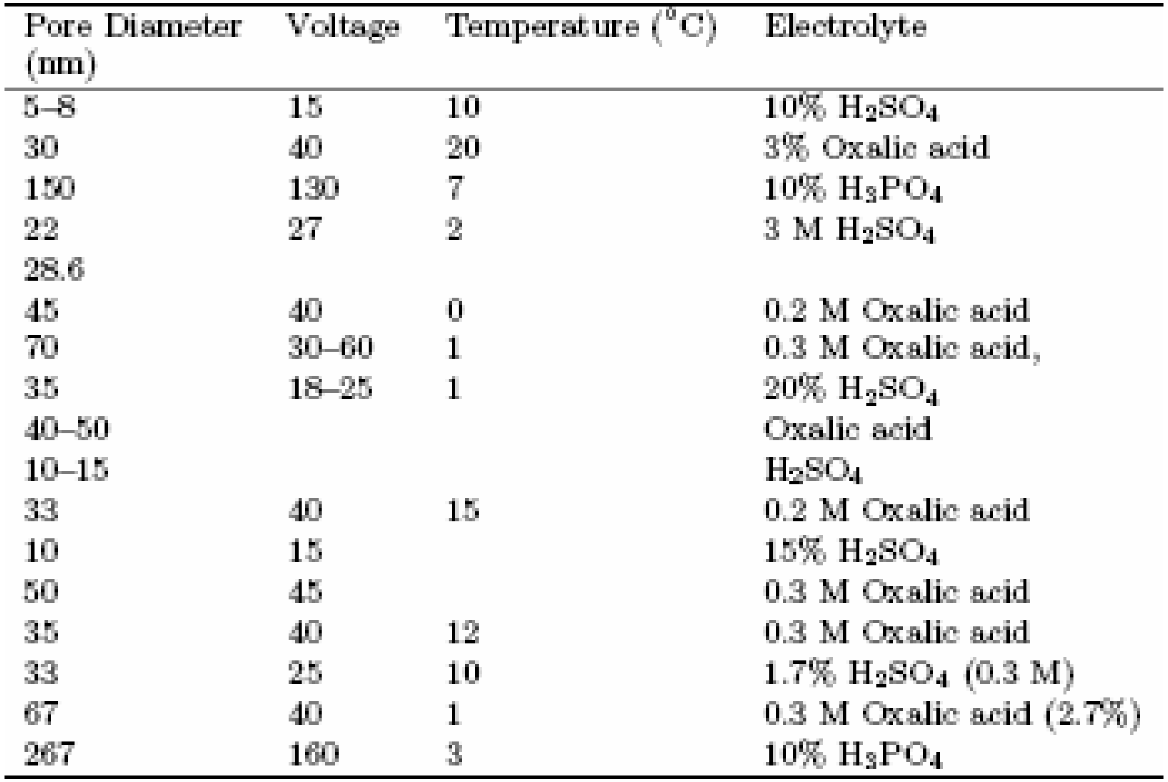
Anodic alumina membranes: self-organisation at nanometric scale





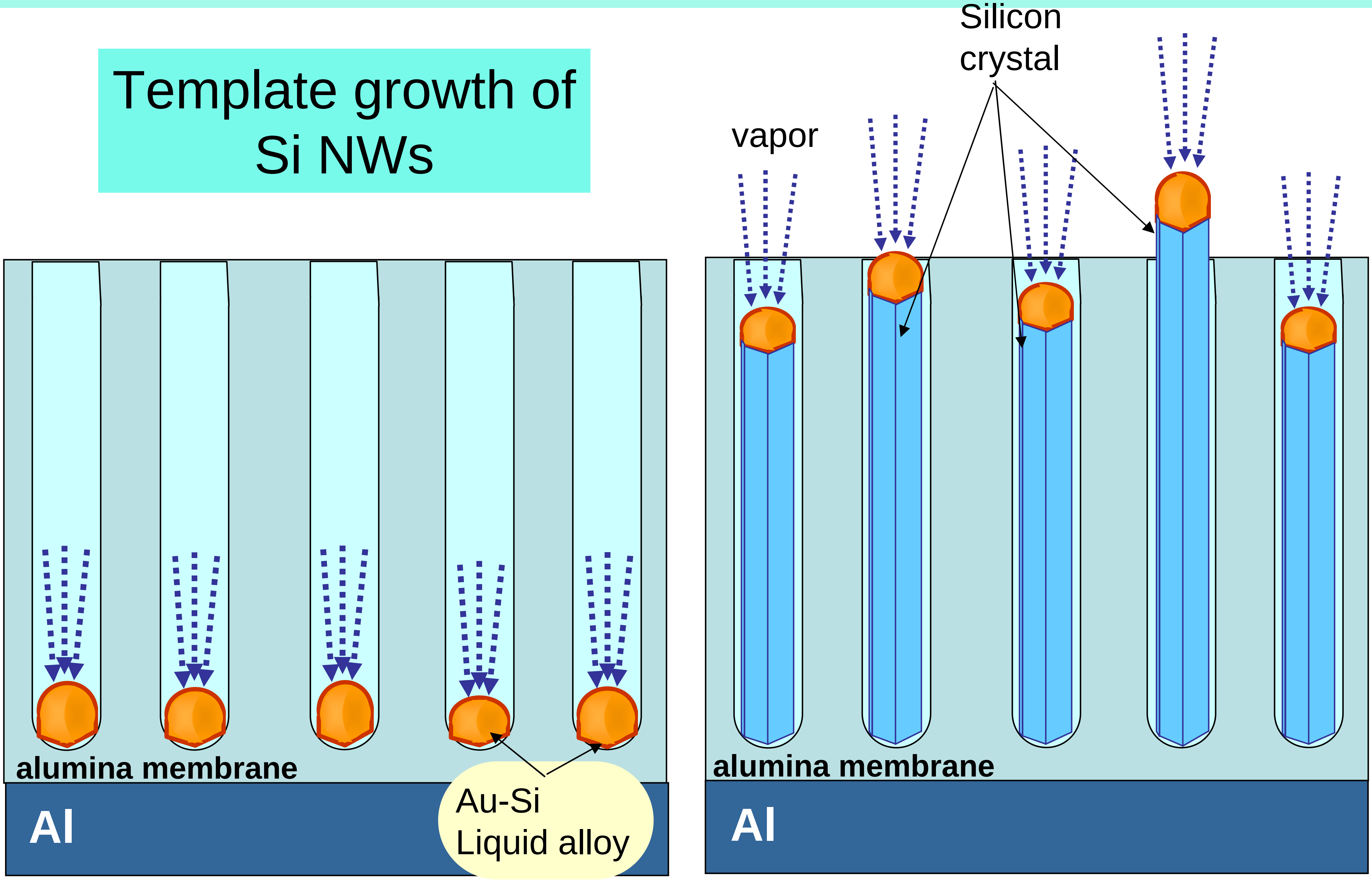




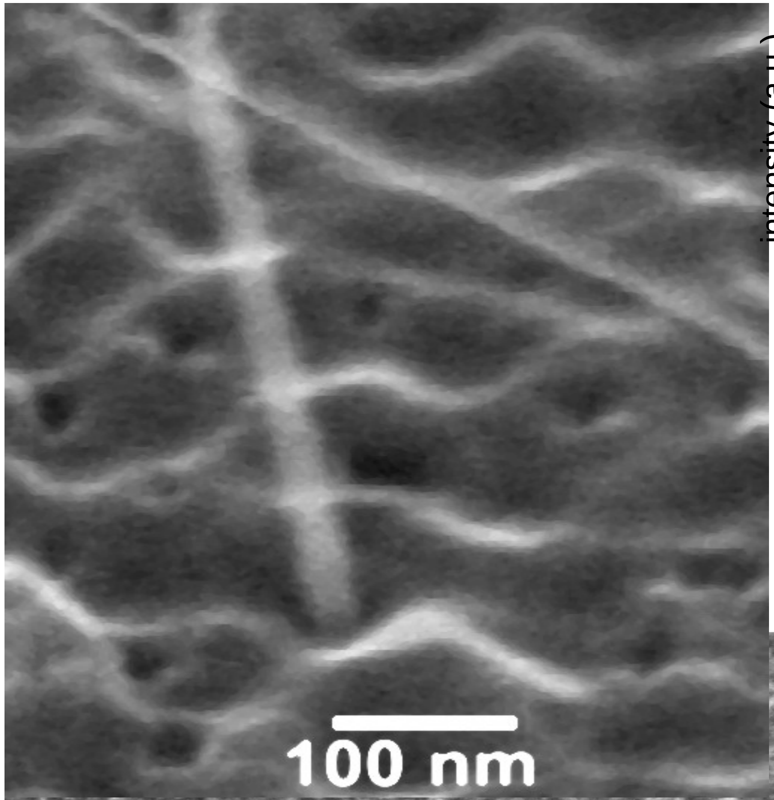


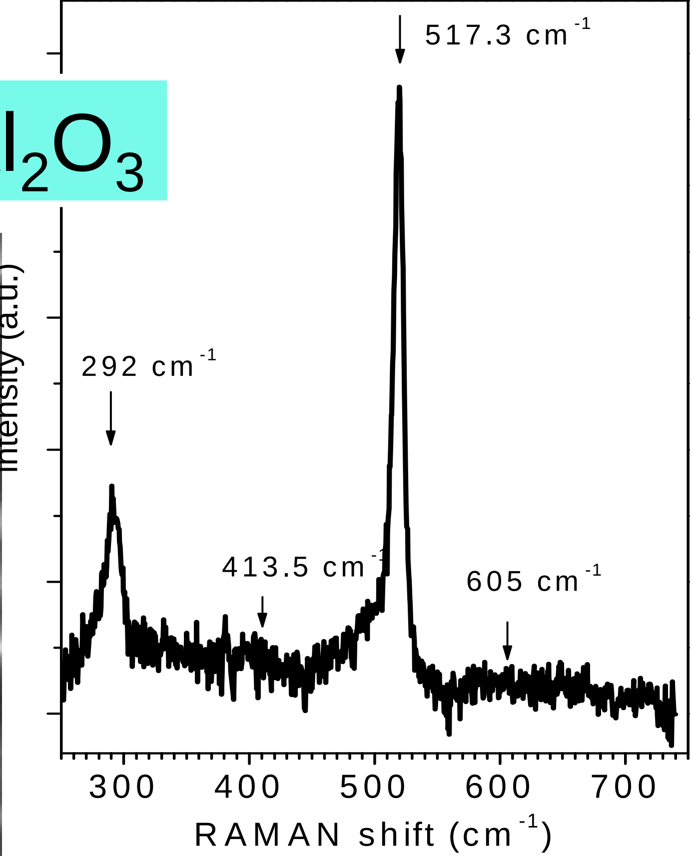
Pore Diameter (nm)	Voltage	Temperature (°C)	Electrolyte
5–8	15	10	10% H_2SO_4
30	40	20	3% Oxalic acid
150	130	7	10% H_3PO_4
22	27	2	3 M H_2SO_4
28.6			
45	40	0	0.2 M Oxalic acid
70	30–60	1	0.3 M Oxalic acid,
35	18–25	1	20% H_2SO_4
40–50			Oxalic acid
10–15			H_2SO_4
33	40	15	0.2 M Oxalic acid
10	15		15% H_2SO_4
50	45		0.3 M Oxalic acid
35	40	12	0.3 M Oxalic acid
33	25	10	1.7% H_2SO_4 (0.3 M)
67	40	1	0.3 M Oxalic acid (2.7%)
267	160	3	10% H_3PO_4

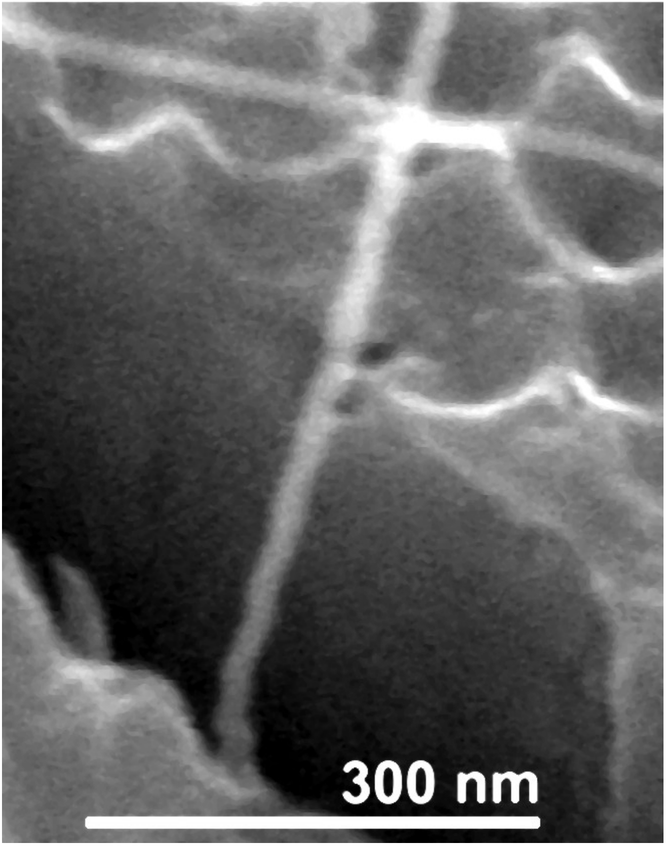
Template growth of Si NWs

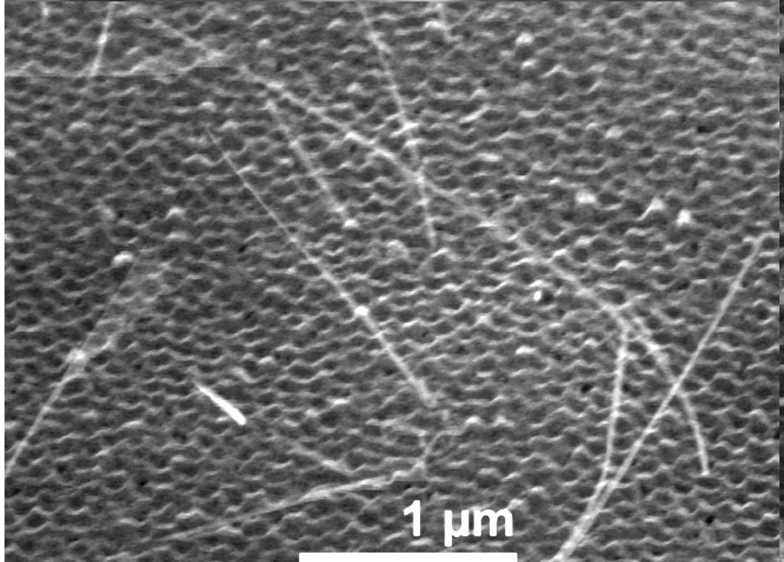


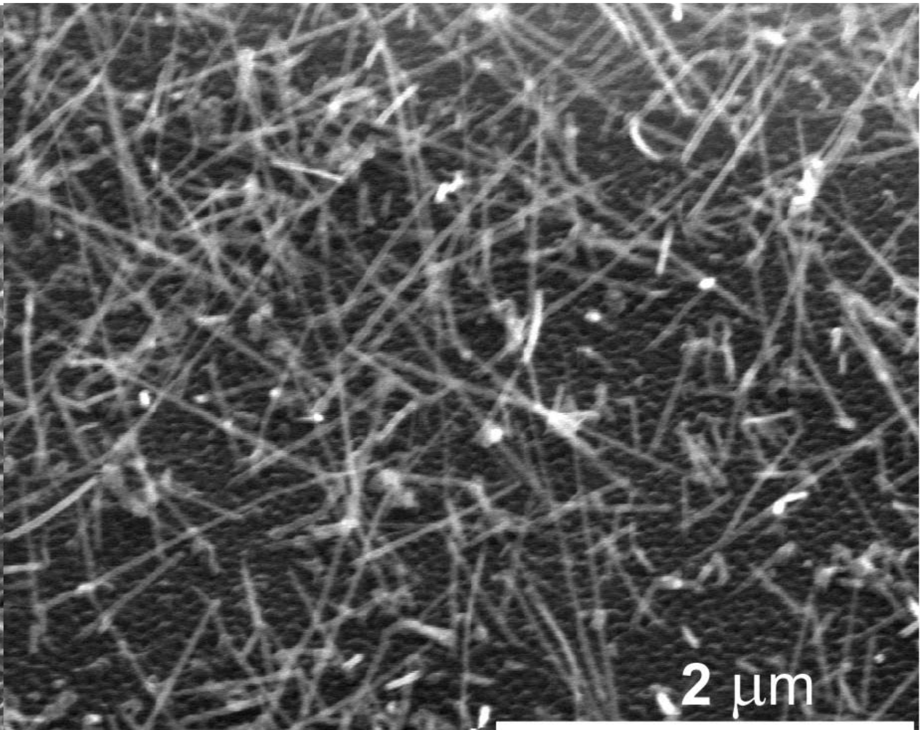
Si NWs in porous Al_2O_3

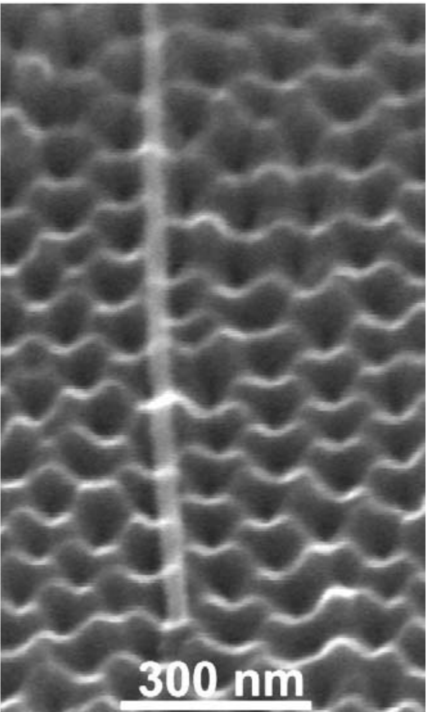




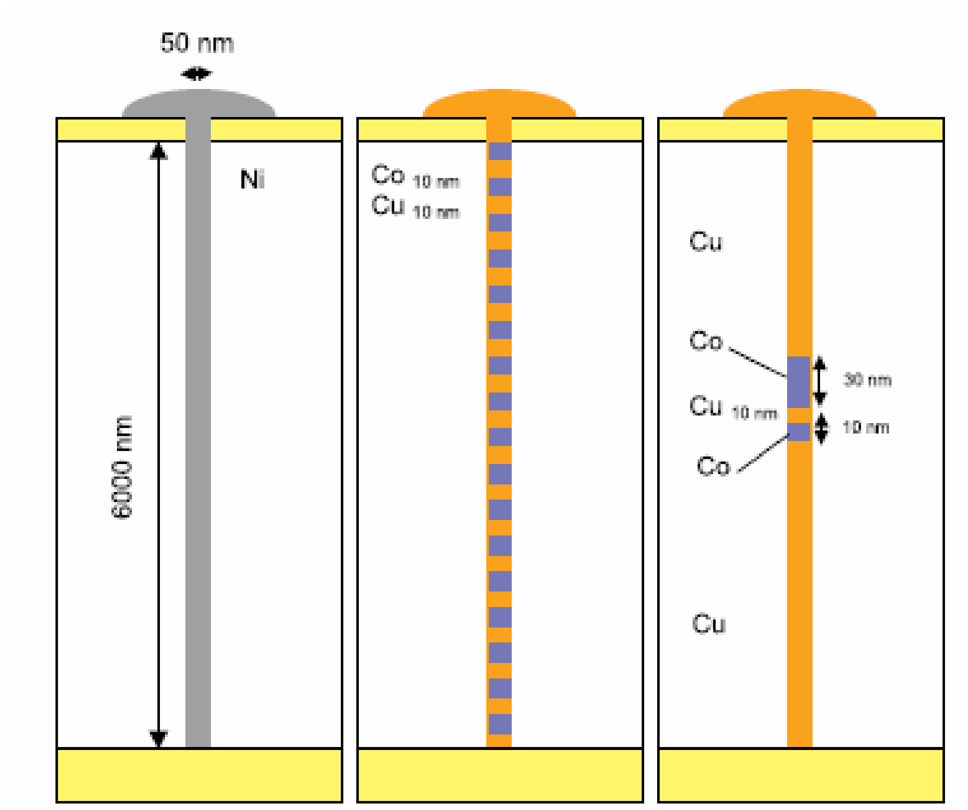




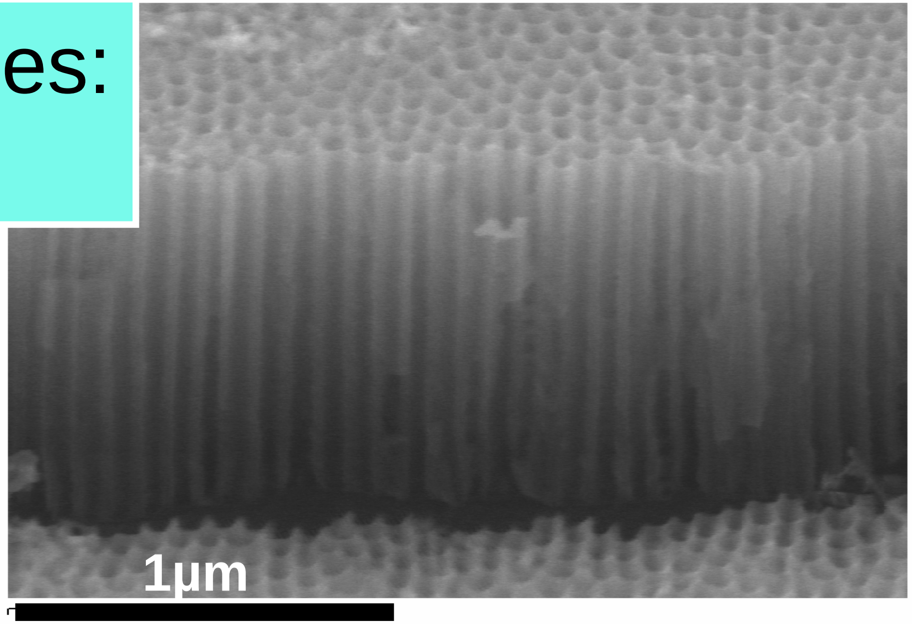


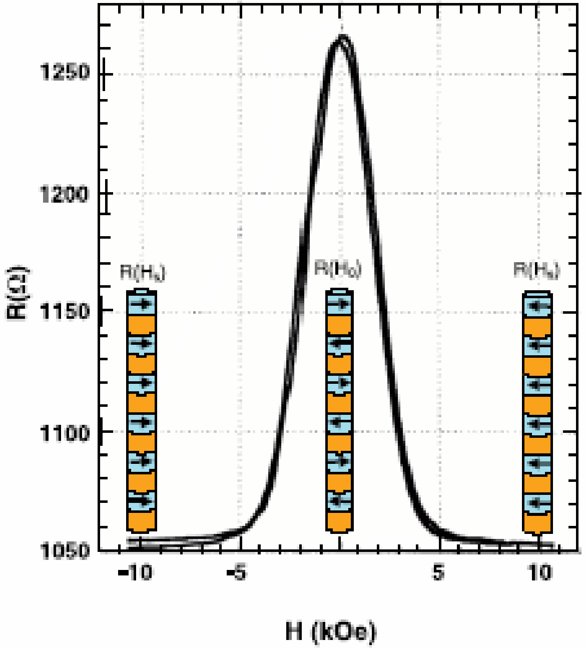


Template-grown nanostructures: OK for two-terminal devices



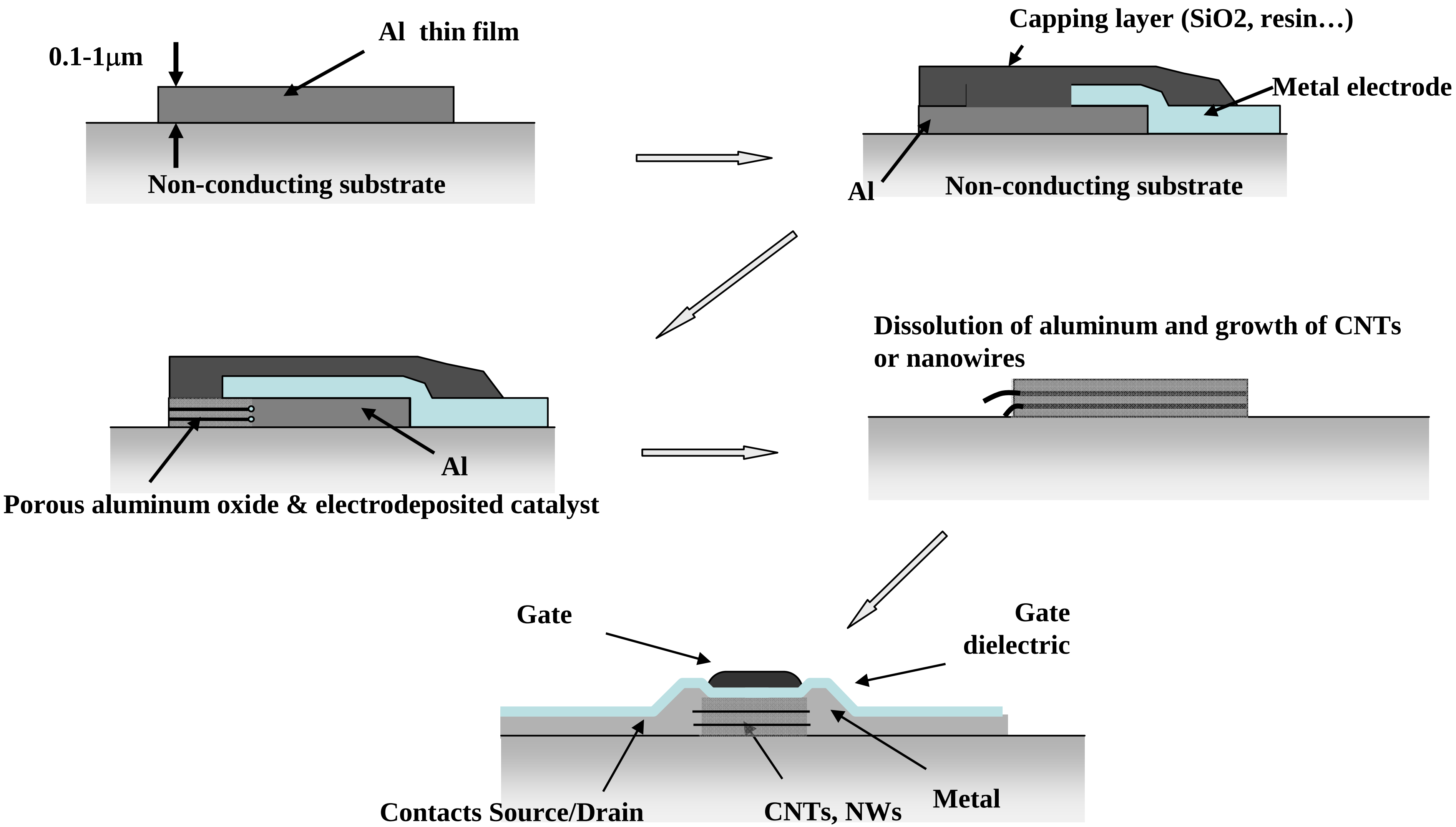
Wade & Wegrowe, *Europ. Phys. J. Appl. Phys. 2005*





Ex : GMR measurements on a Co/Cu nw

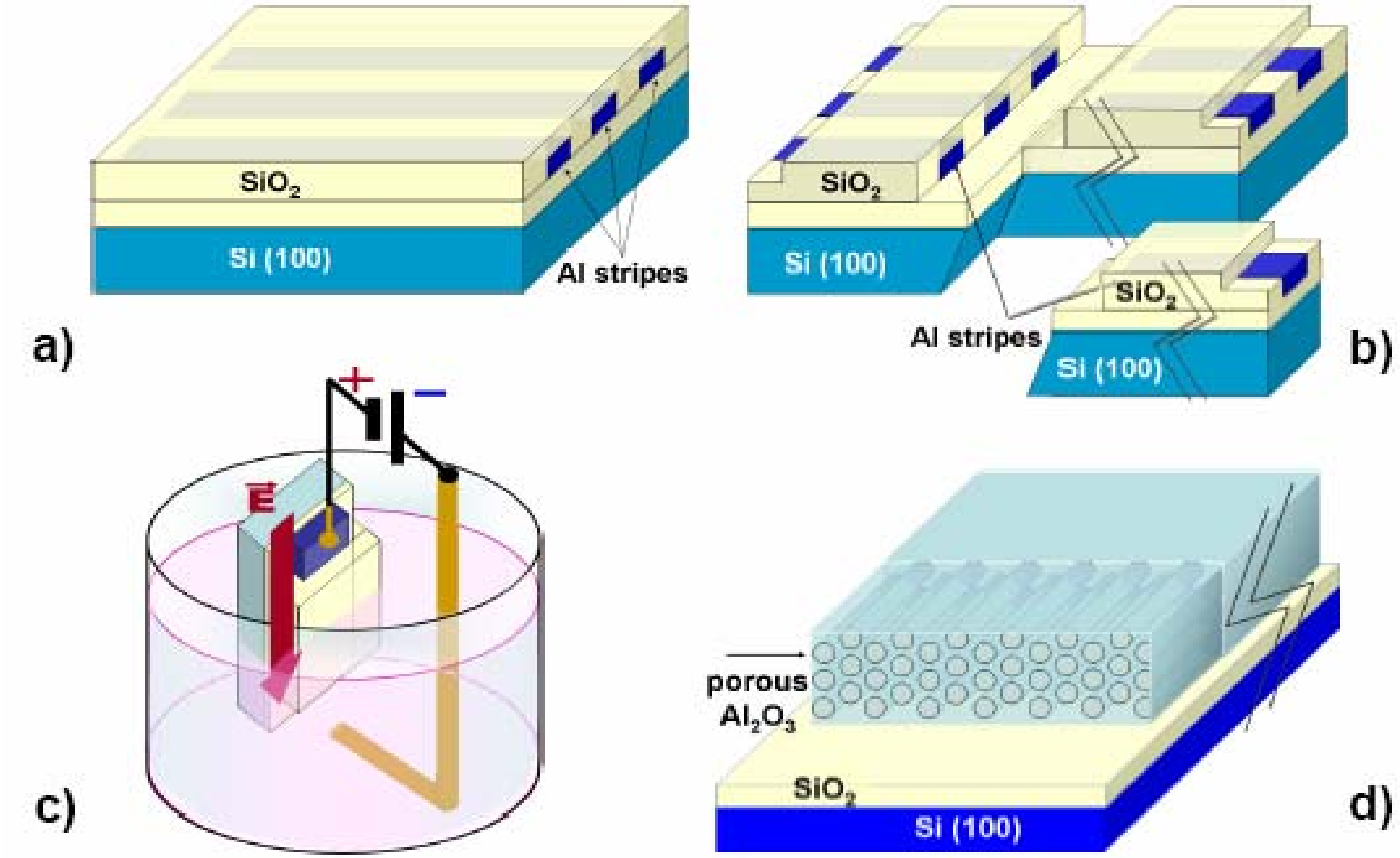
Template growth in lateral porous anodic Al_2O_3 films



Nano Lett., Vol. 5, No. 4, 2005
CNRS patent FR 03 11959

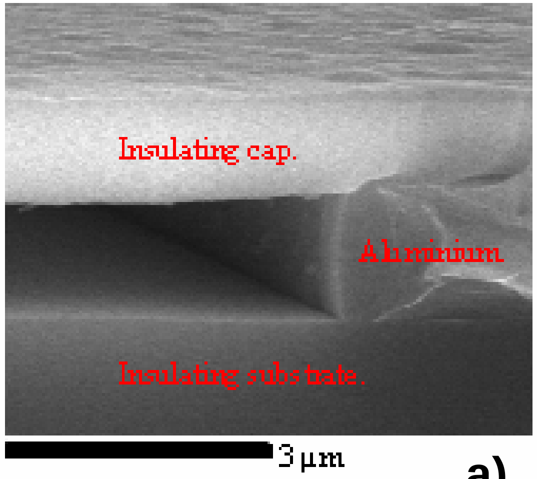
D. Pribat

Template growth in lateral porous anodic Al_2O_3 films

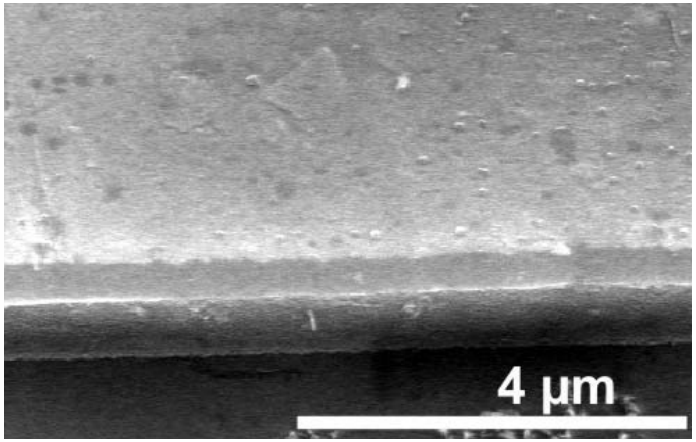


Nano Lett., Vol. 5, No. 4, 2005
CNRS patent FR 03 11959

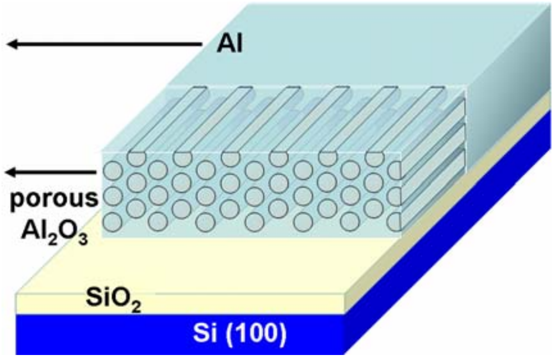
SEM characterisations of lateral Al_2O_3 membranes

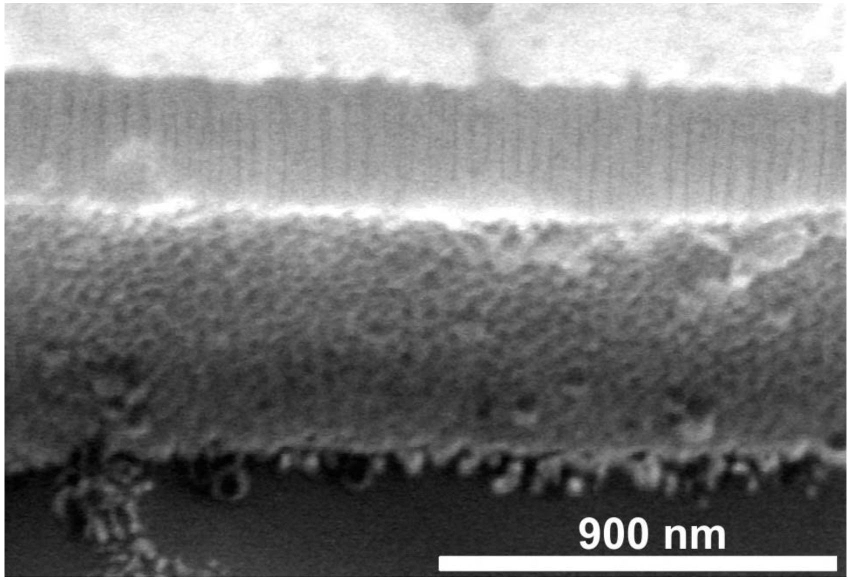


a)

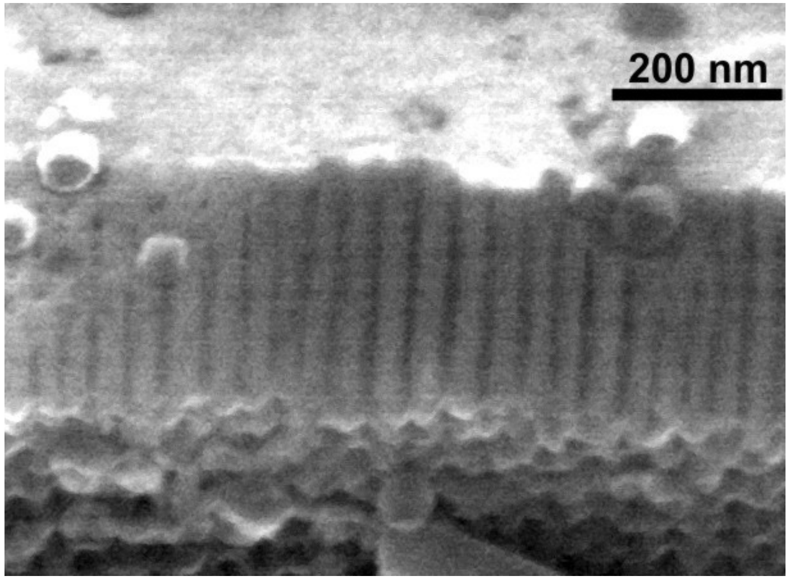


b)



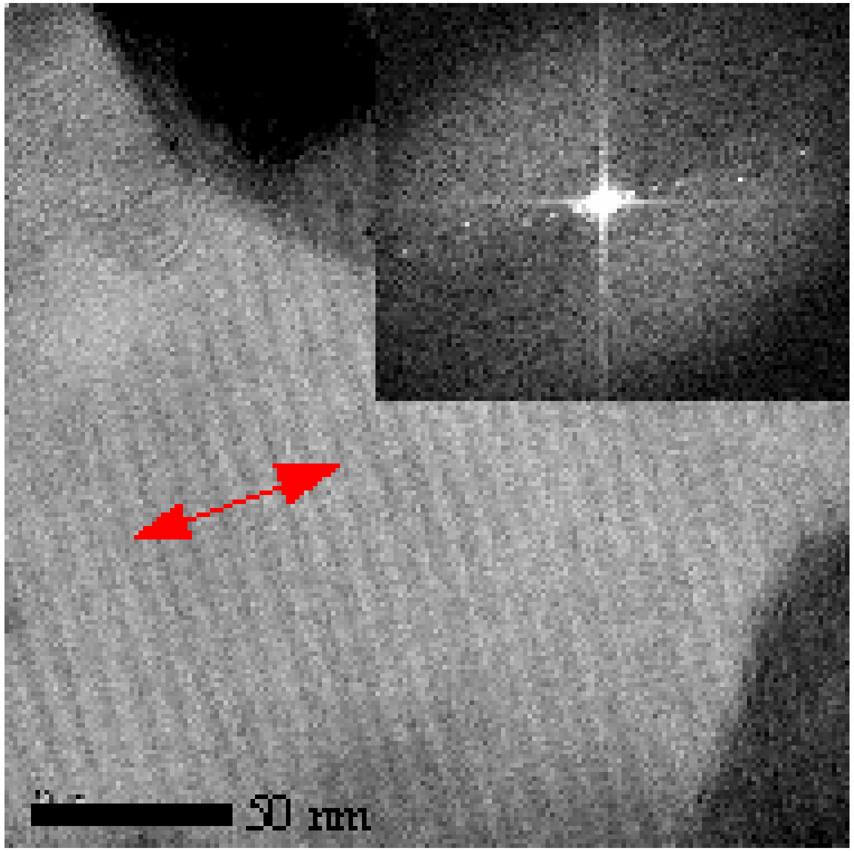


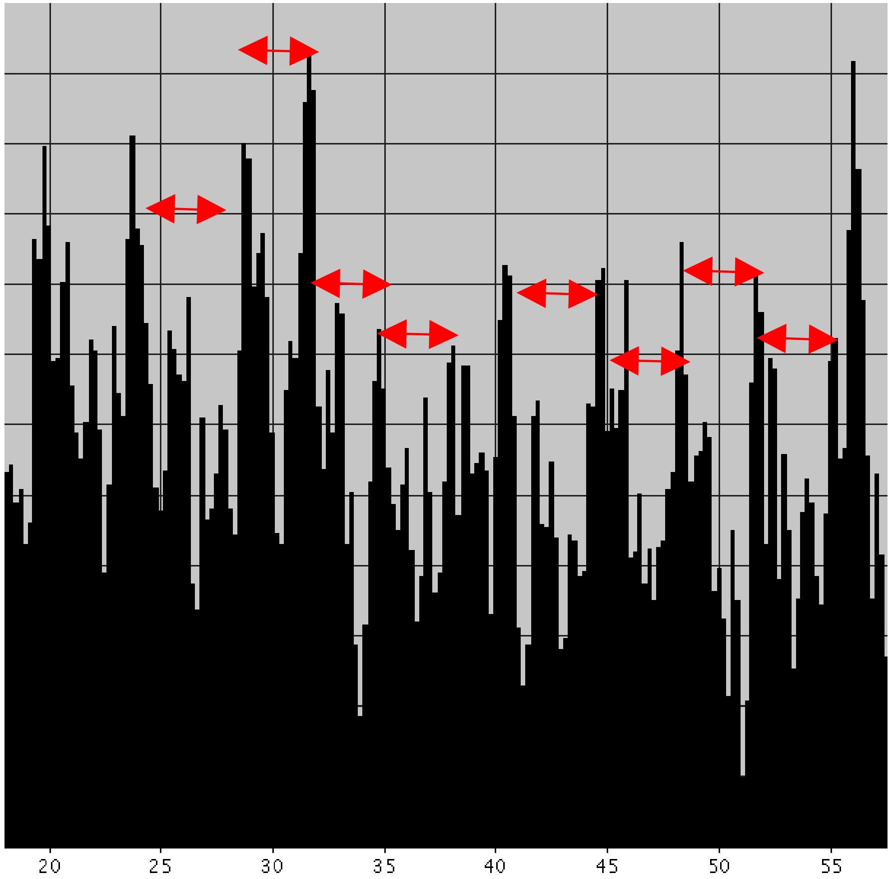
c)



d)

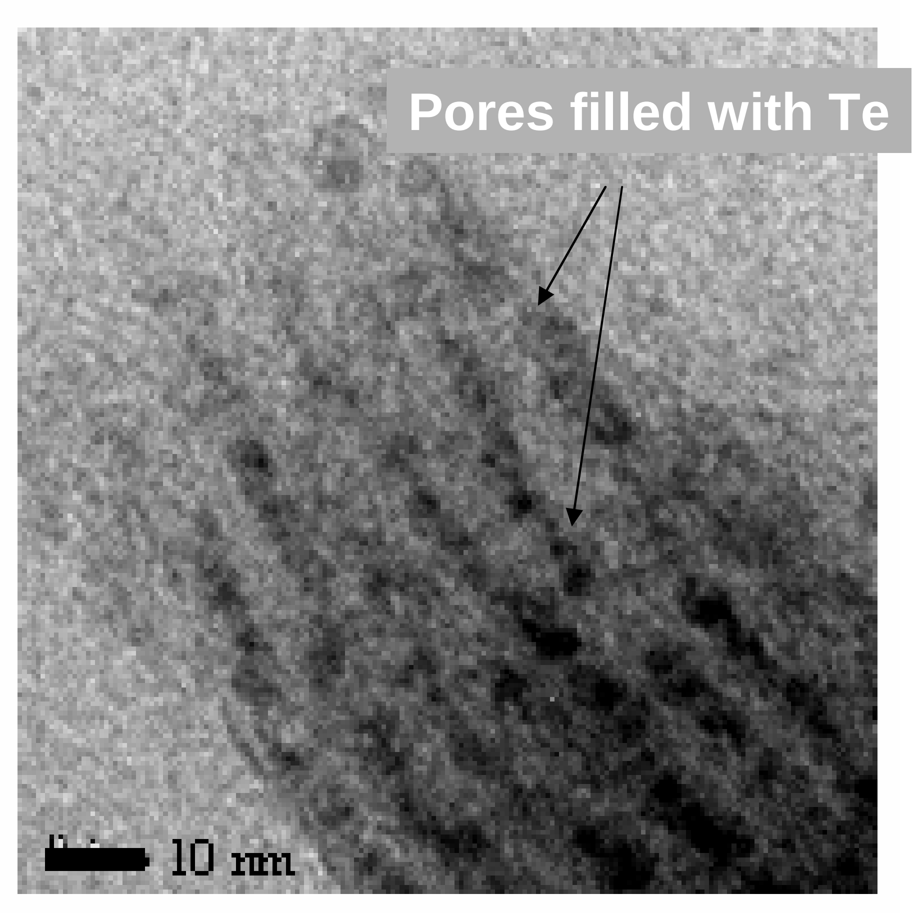
TEM characterisations of lateral Al_2O_3 membranes (1)

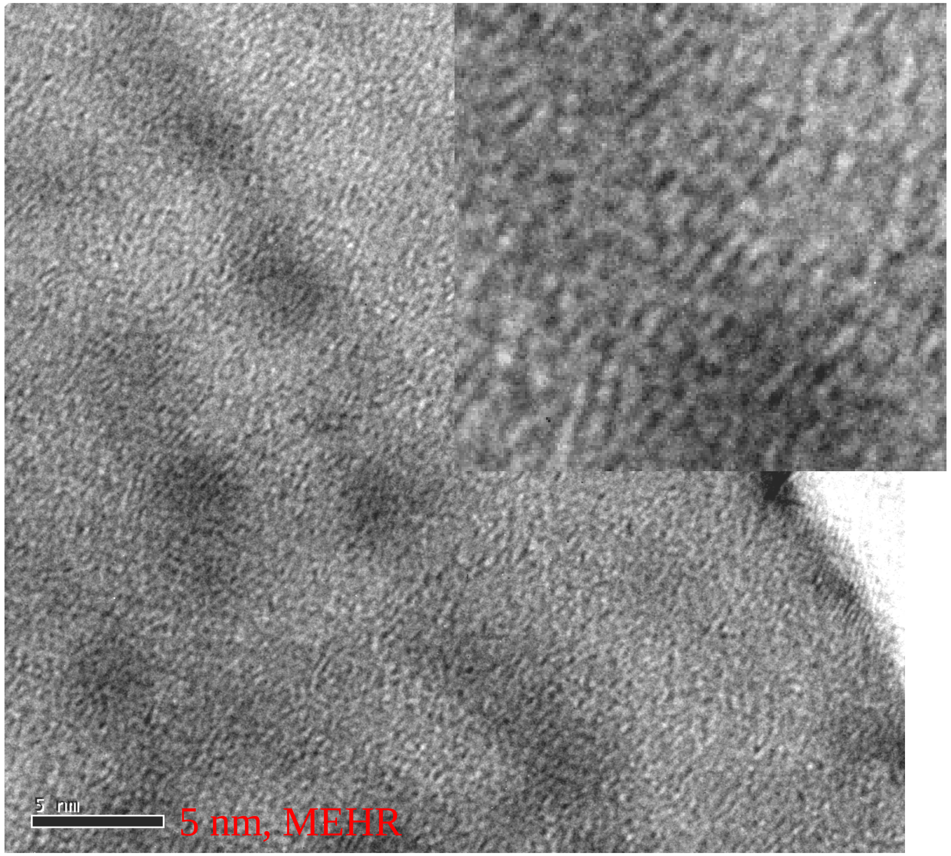




The red bars represent 3.5 nm

TEM characterisations of lateral membranes (2)





ÉCOLE POLYTECHNIQUE

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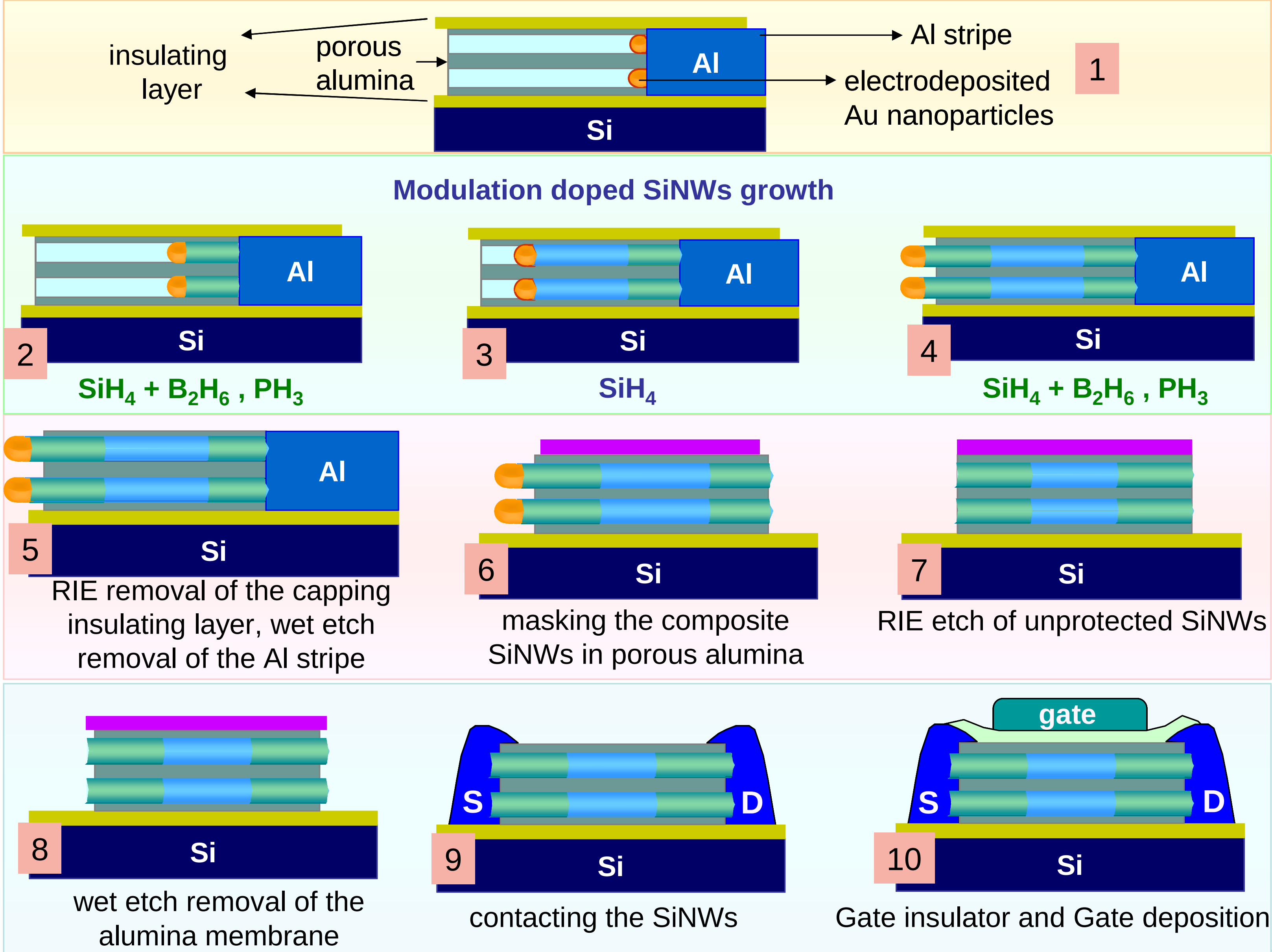
Transistor fabrication with sequential doping



Modulation doped SiNWs growth

$SiH_4 + B_2H_6$, PH_3

SiH_4

$SiH_4 + B_2H_6$, PH_3

RIE removal of the capping insulating layer, wet etch removal of the Al stripe

masking the composite SiNWs in porous alumina

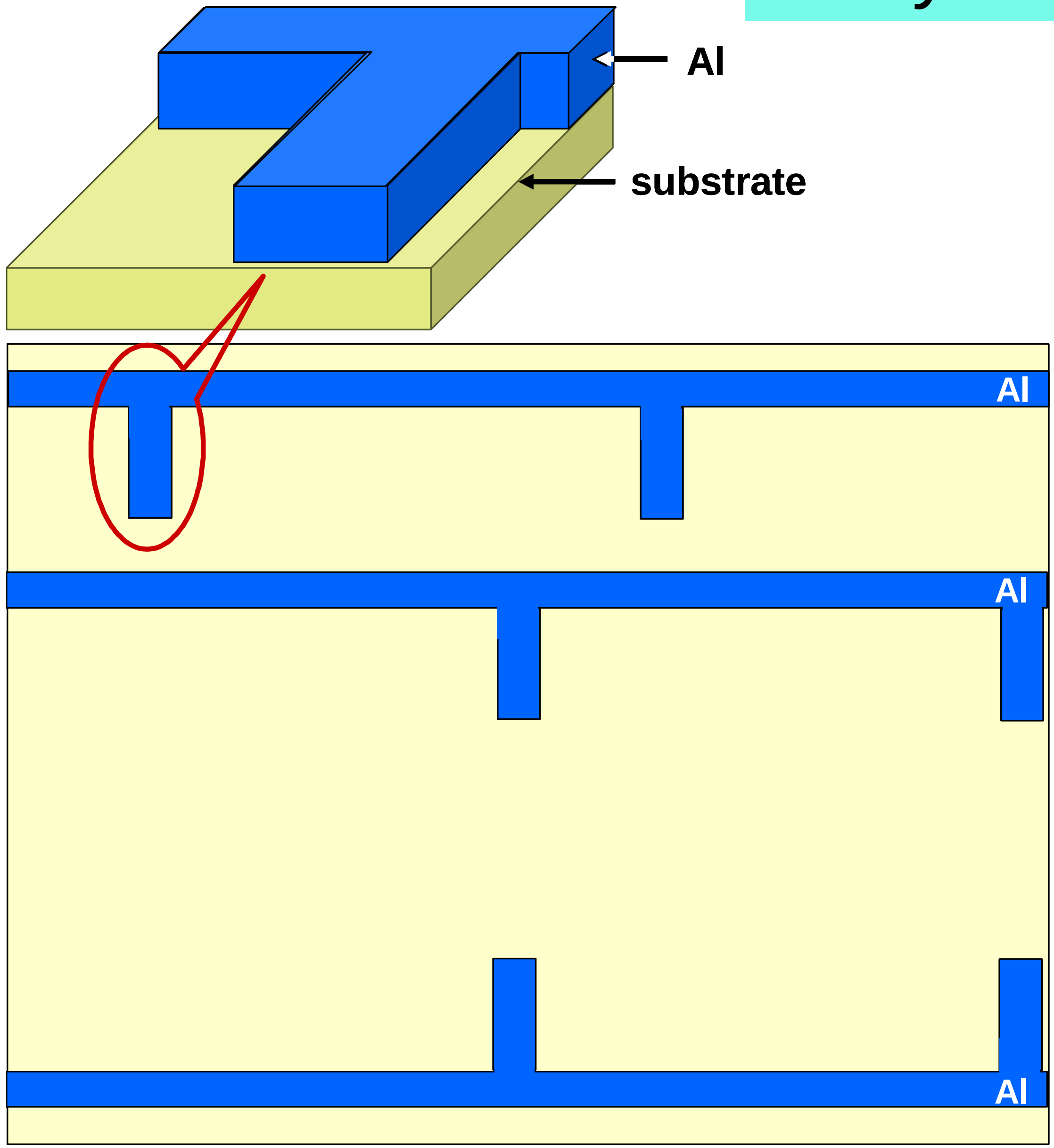
RIE etch of unprotected SiNWs

wet etch removal of the alumina membrane

contacting the SiNWs

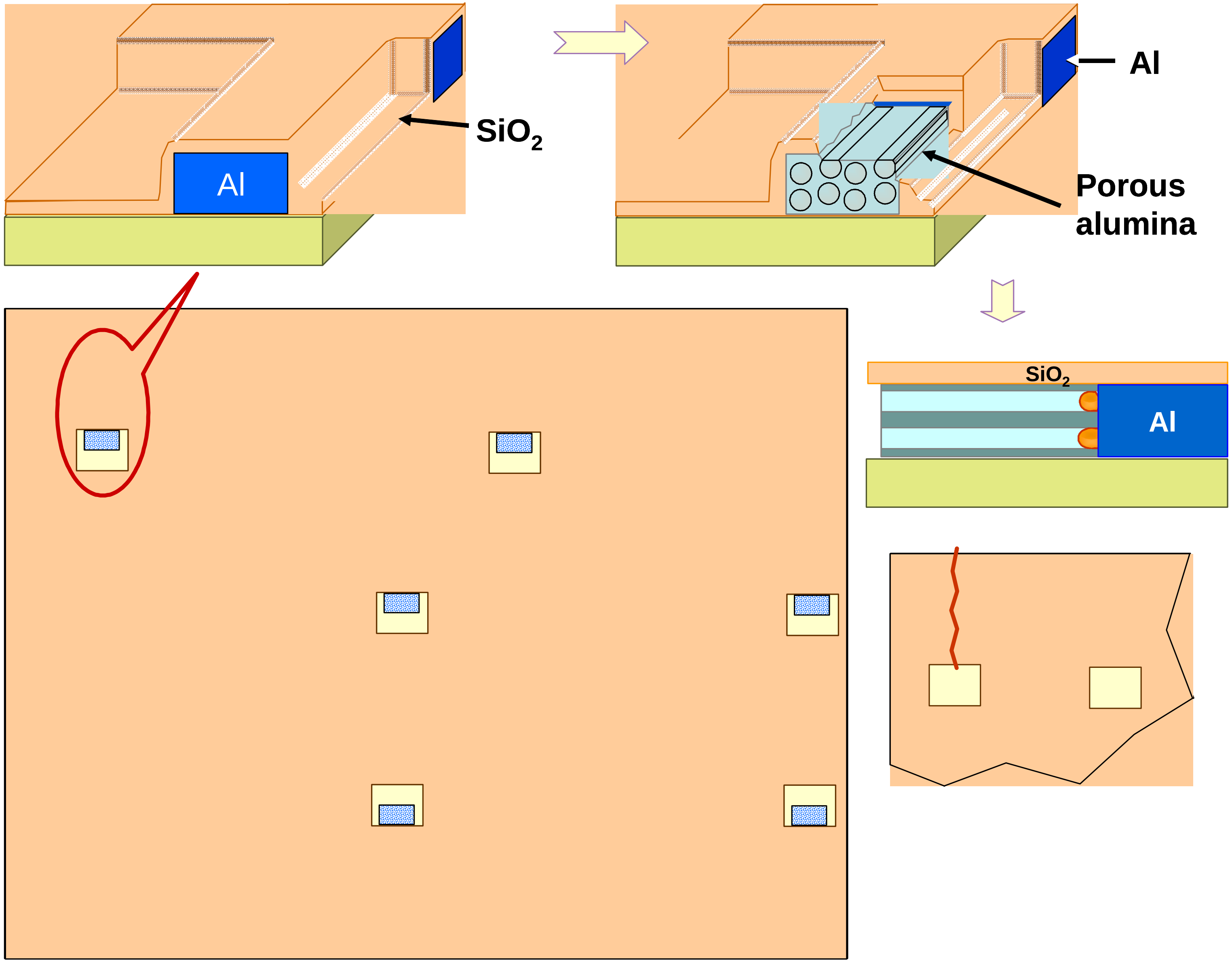
Gate insulator and Gate deposition

Array with a 5-mask process (1)



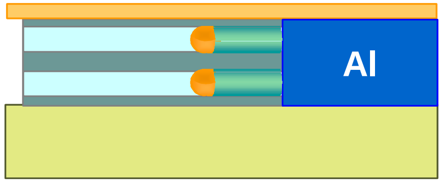
Mask # 1
Al etching

Array with a 5-mask process (2)

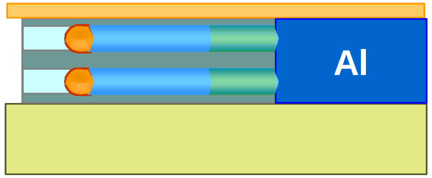


SiO$_2$ deposition
+
Mask # 2
+
Anodic oxidation
+
Catalyst electrodep.

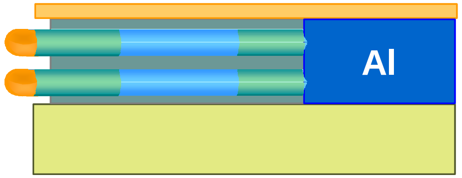
Array with a 5-mask process (3)



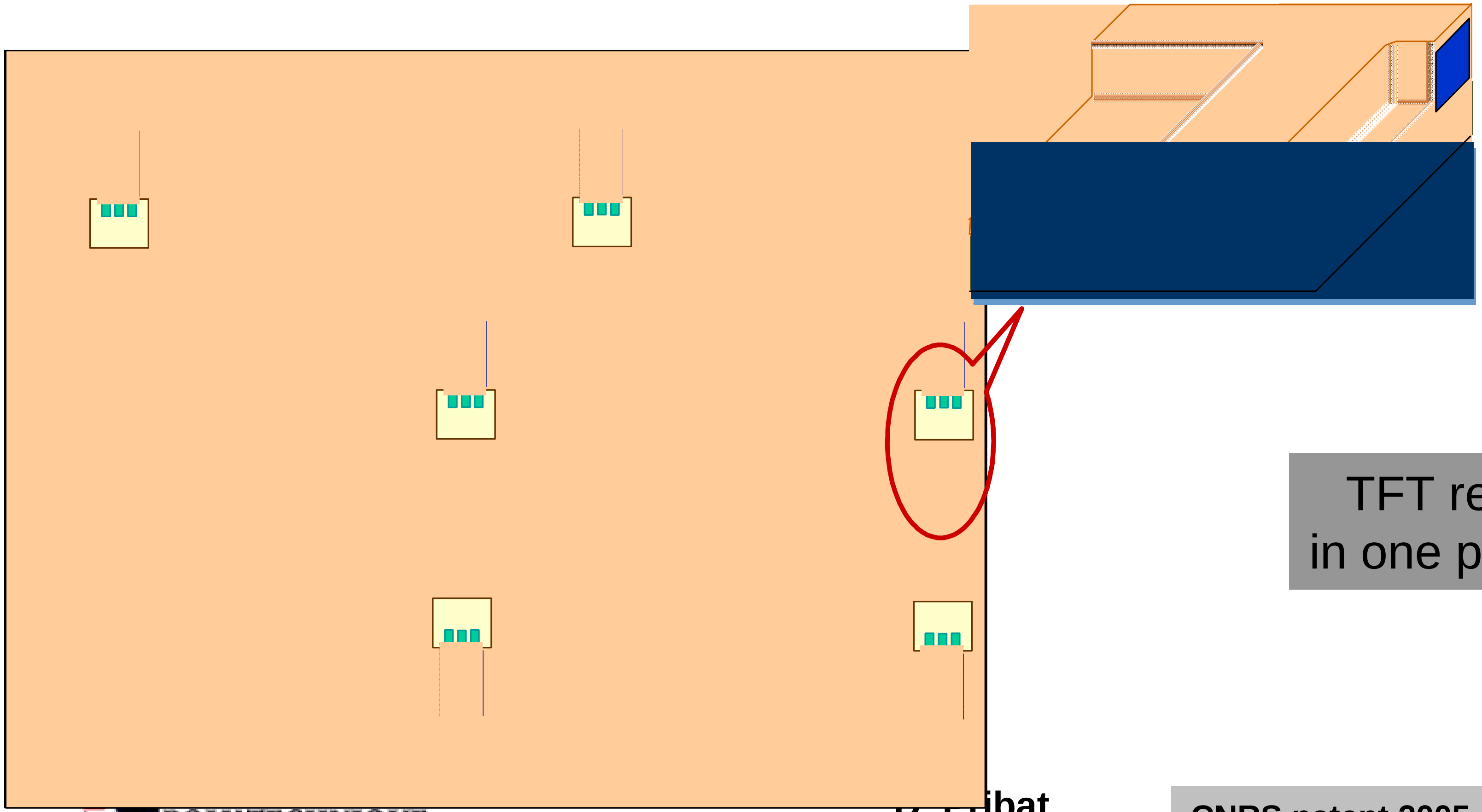
$SiH_4 + B_2H_6$, PH_3



SiH_4



$SiH_4 + B_2H_6$, PH_3

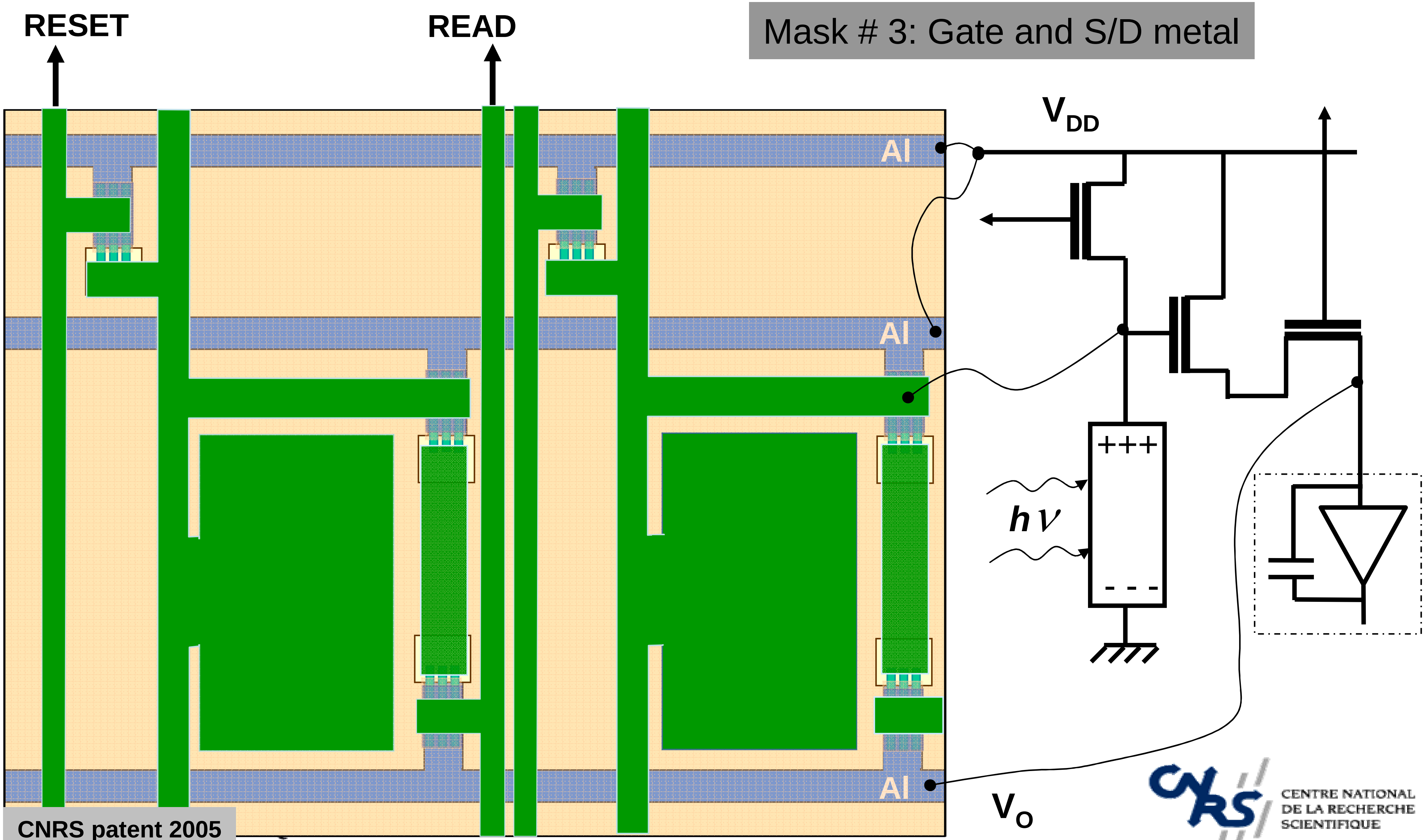


TFT realisation
in one pump down

CNRS patent 2005

Array with a 5-mask process (4)

Mask # 3: Gate and S/D metal



CNRS patent 2005

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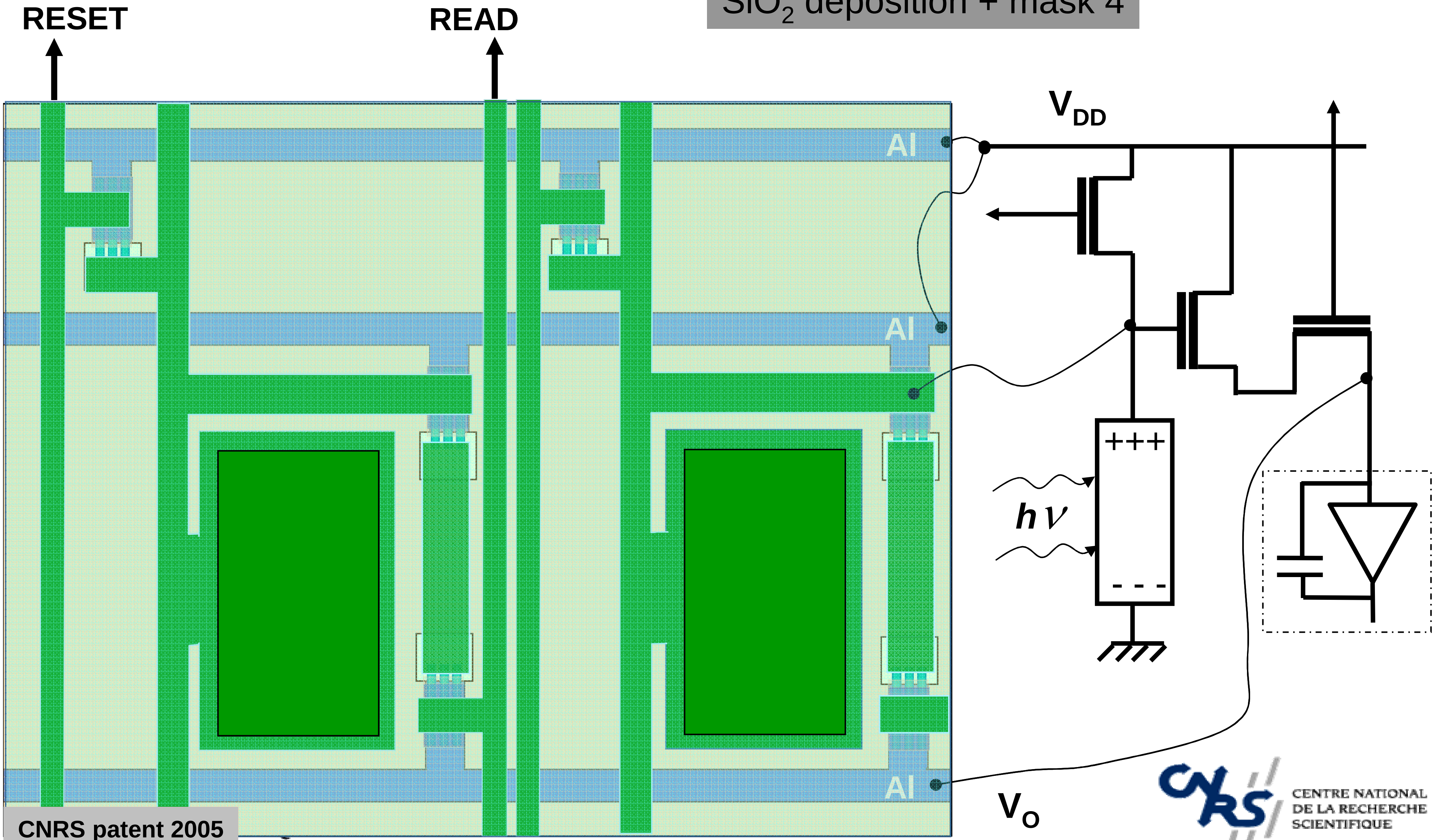
Array with a 5-mask process (5)

SiO_2 deposition + mask 4



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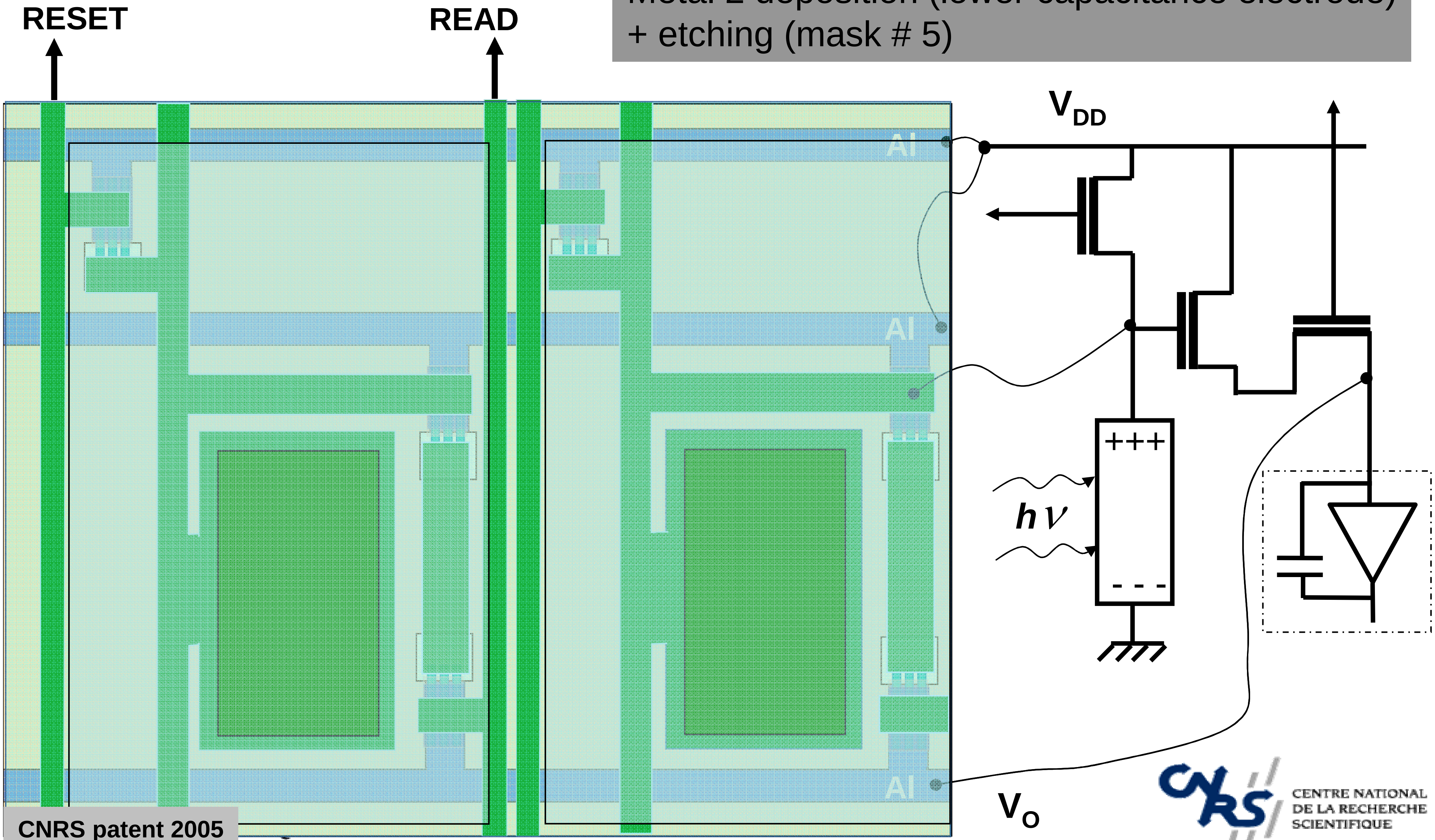
Array with a 5-mask process (6)

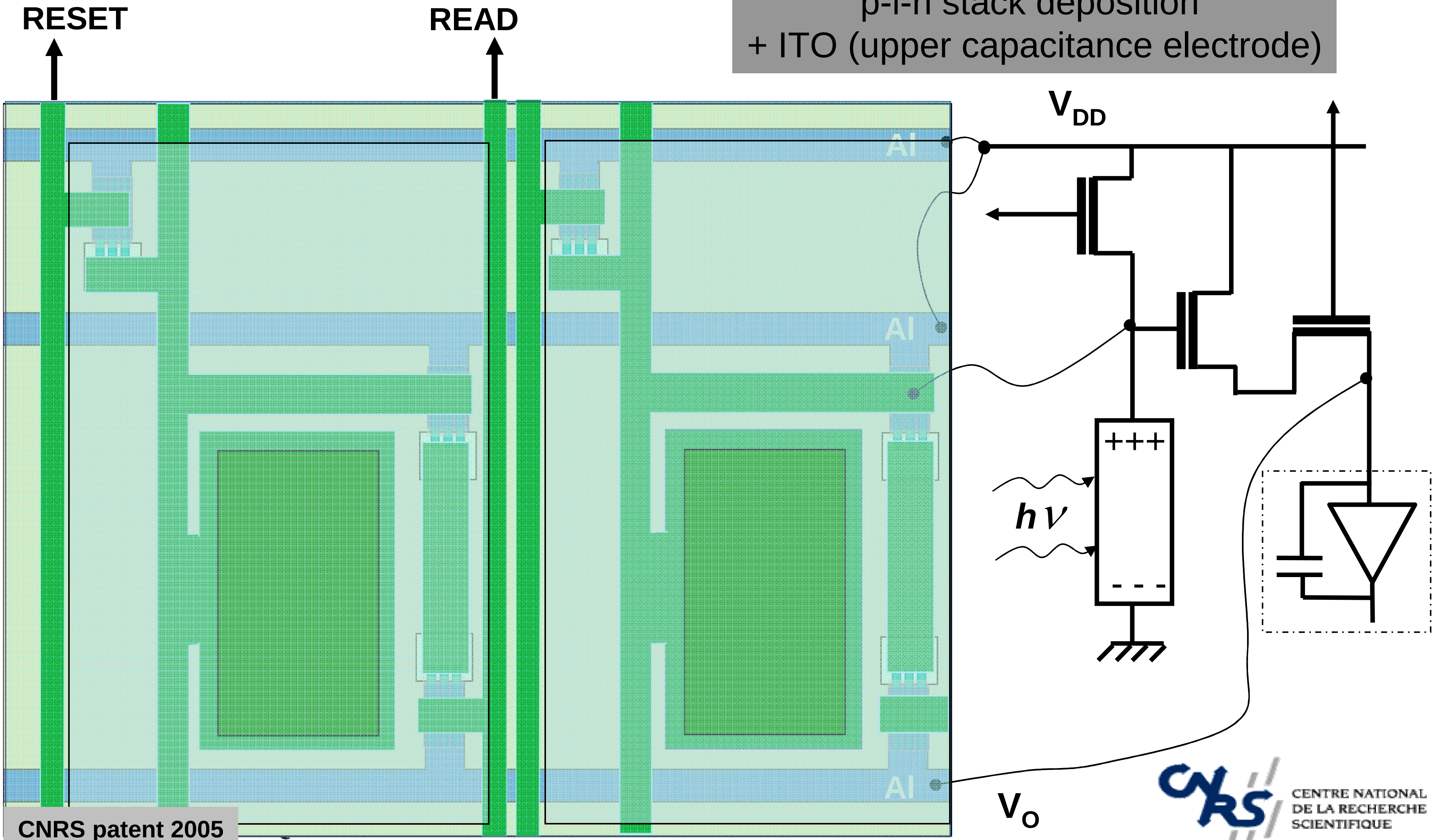
Metal 2 deposition (lower capacitance electrode) + etching (mask # 5)



CNRS patent 2005

Array with a 5-mask process (7)

p-i-n stack deposition
+ ITO (upper capacitance electrode)



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SCIENTIFIQUE

Conclusions

- a-Si:H-based imagers present a number of advantages
  - Large size, high resolution, high image quality
  - Electronic picture handling
  - Compactness
  - Synergy with AMLCD industry (equipment, technologies…)
  - ….
- Need for added pixel complexity
  - a-Si:H limitations
- Alternative technologies
  - Poly-Si: complex (laser), not mature. Niche applications in displays
  - Si NWs: simple, only CVD. Currently being developed