

New Counting ASIC for X-Ray Imaging Devices

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- ASIC objectives
- Pixel and matrix global schematics
- preamplifier schematics
- electrical test results
- future work
- Conclusions

ASIC objectives

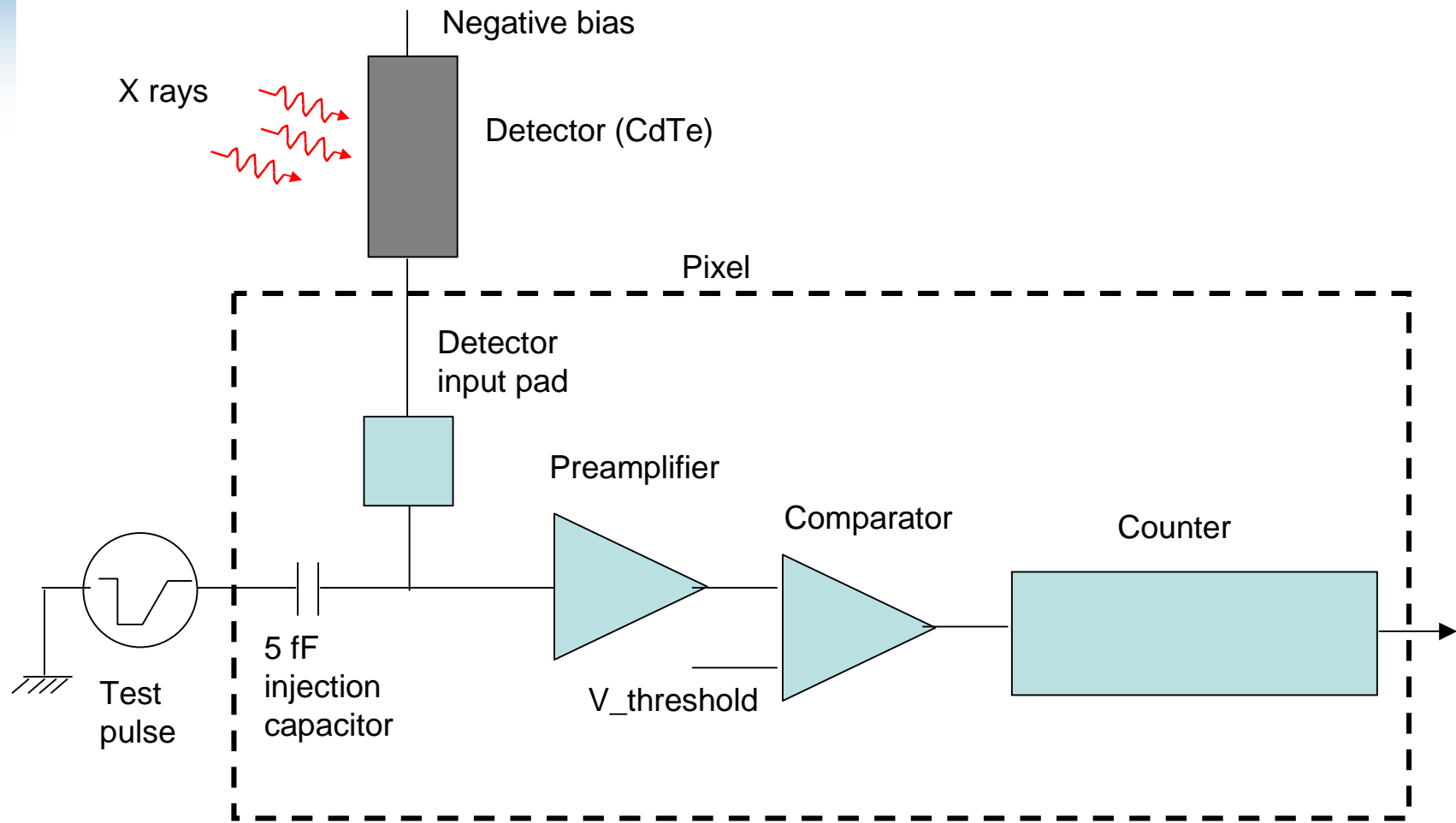
Main objective was to study a new preamplifier schematics for an X ray counting ASIC.

Thus, a very simple test matrix was designed, only including the very basic elements of a counting ASIC

Measurement objectives :

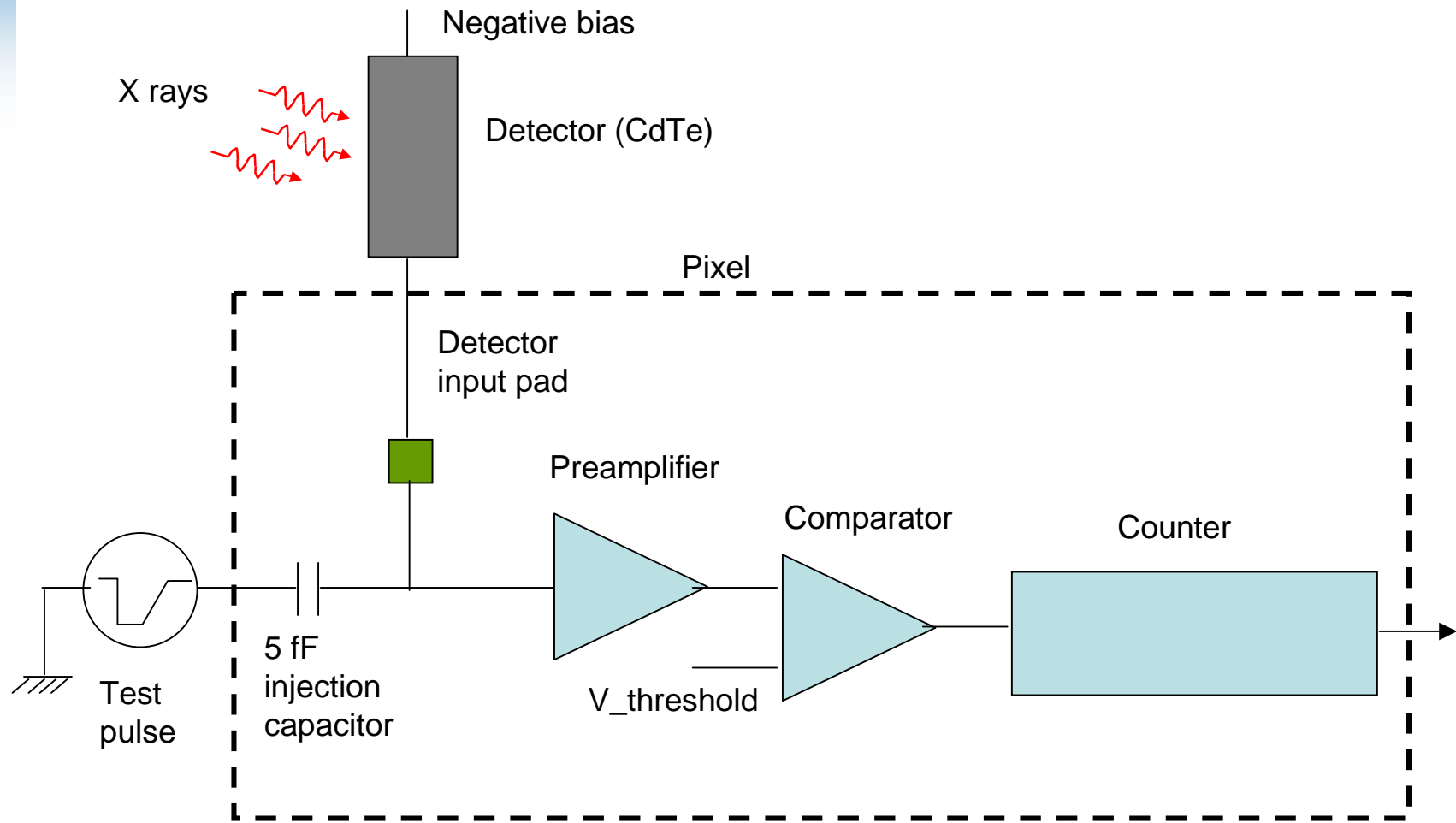
- electrical characterization (this talk)
- Coupling the ASIC to a pixelated photoconductor (namely CdTe or CdZnTe), (future work)

Pixel schematics



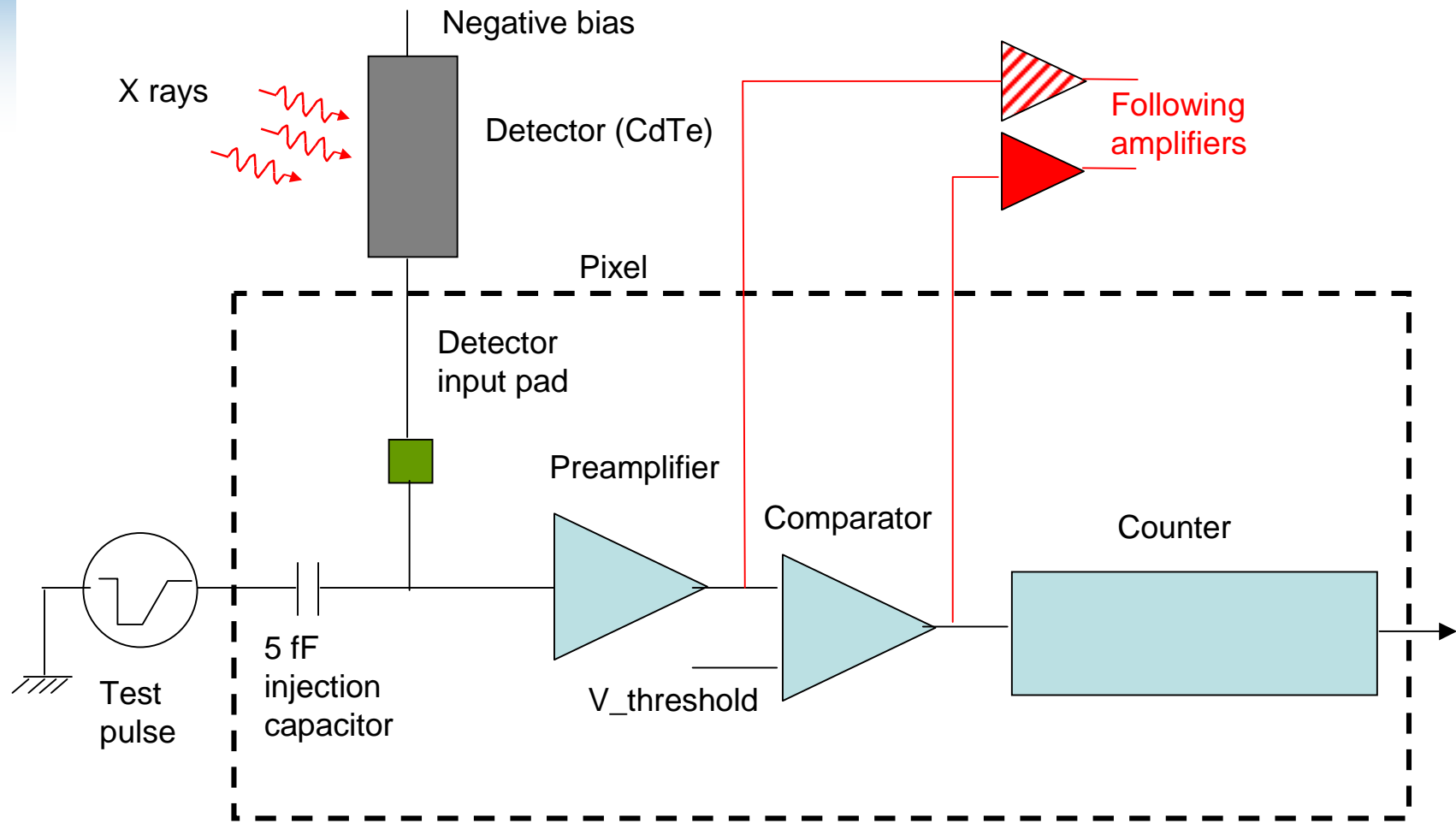
The pixel schematics only includes the basic functions

Pixel schematics : variation of the input pad



2 kinds of pixels differ from the input pad surface (i.e. capacitance) : $30\mu\text{m} \times 30\mu\text{m}$ and $15\mu\text{m} \times 15\mu\text{m}$.

Schematics of the 2 pixels equipped with analog outputs



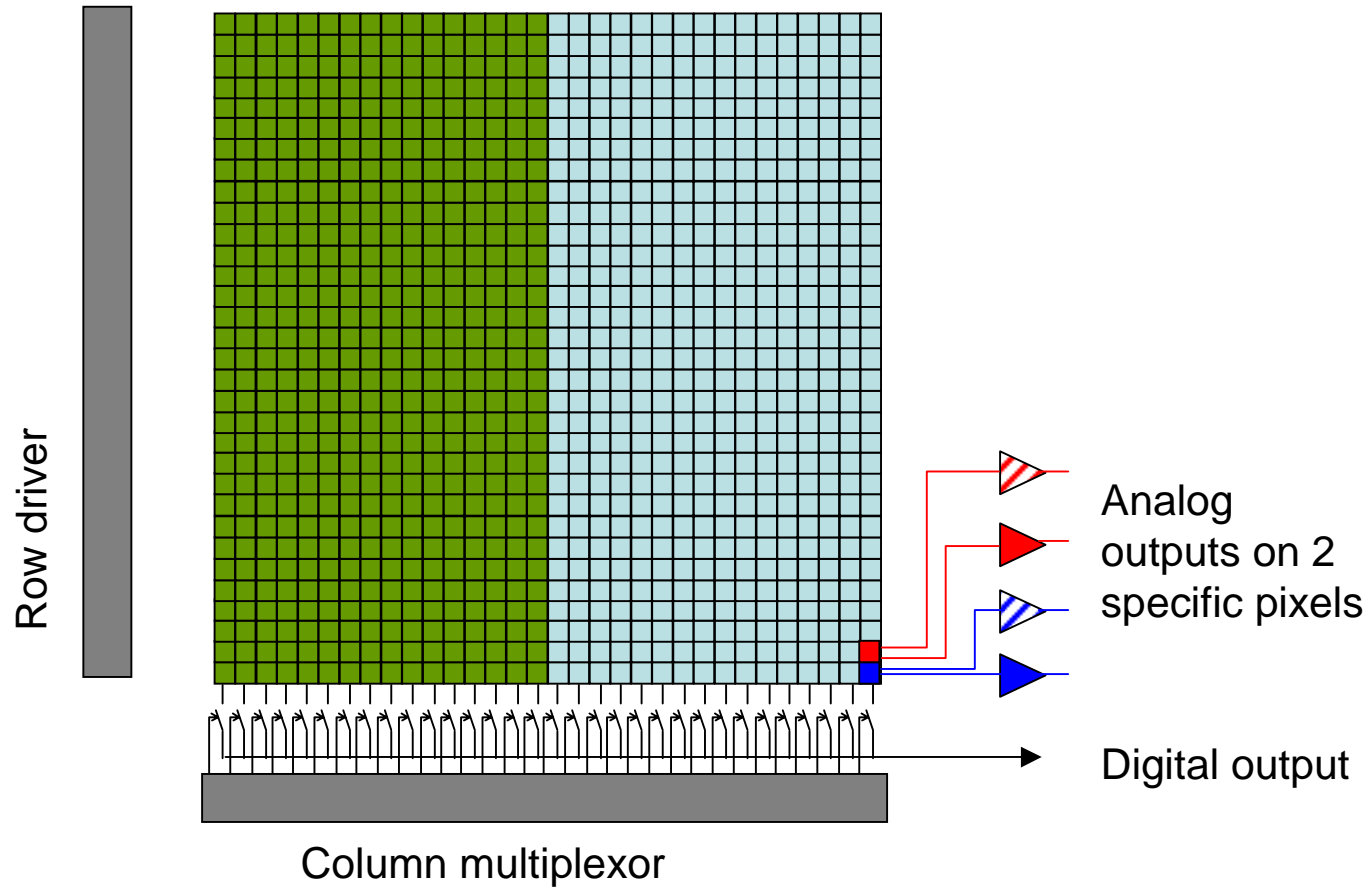
The pixel schematics includes 2 sizes for the detector input pad.

Matrix schematics

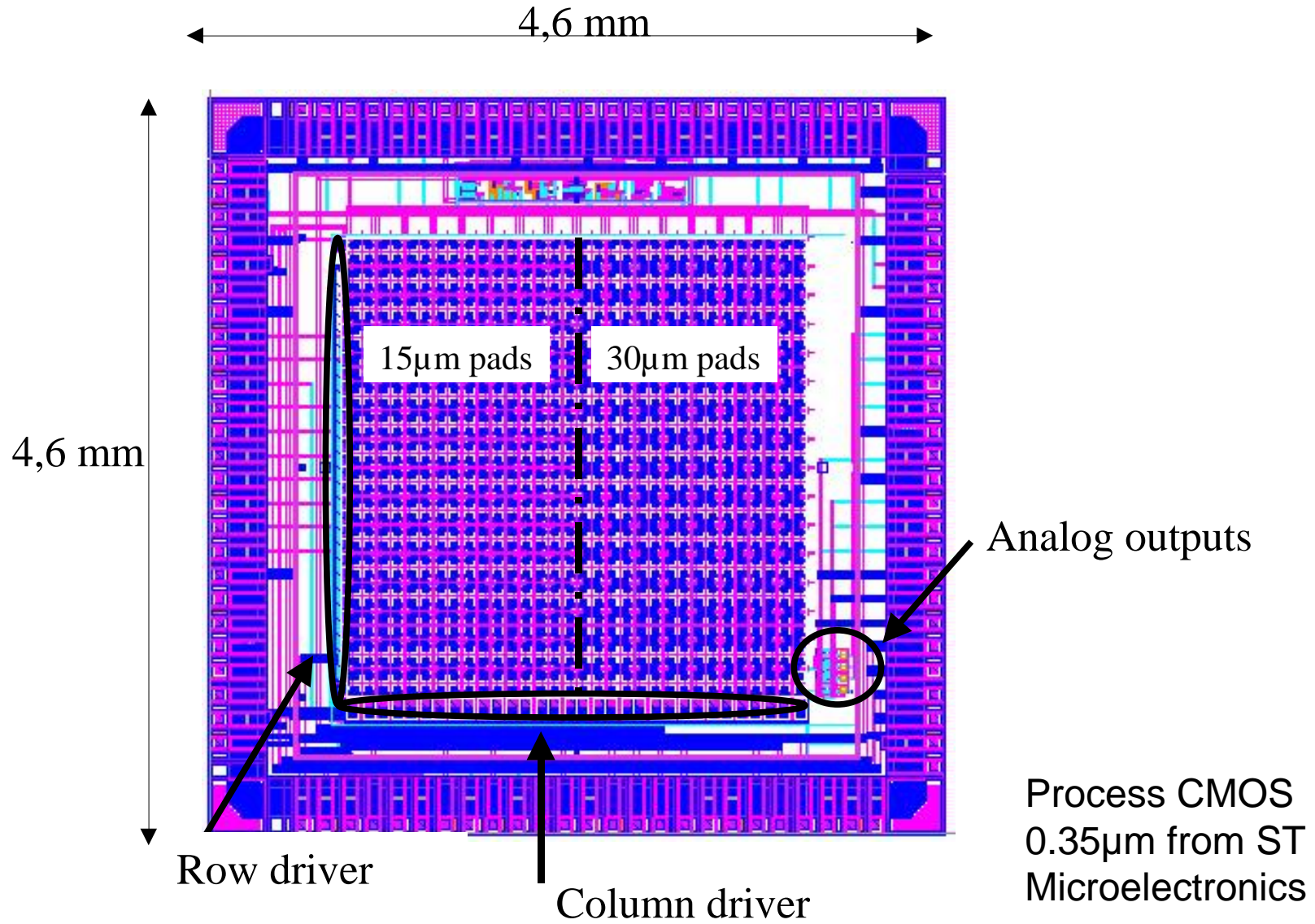
32 x 32 pixel test matrix : 90µm x 90µm pixels

Half of the matrix with small input pads

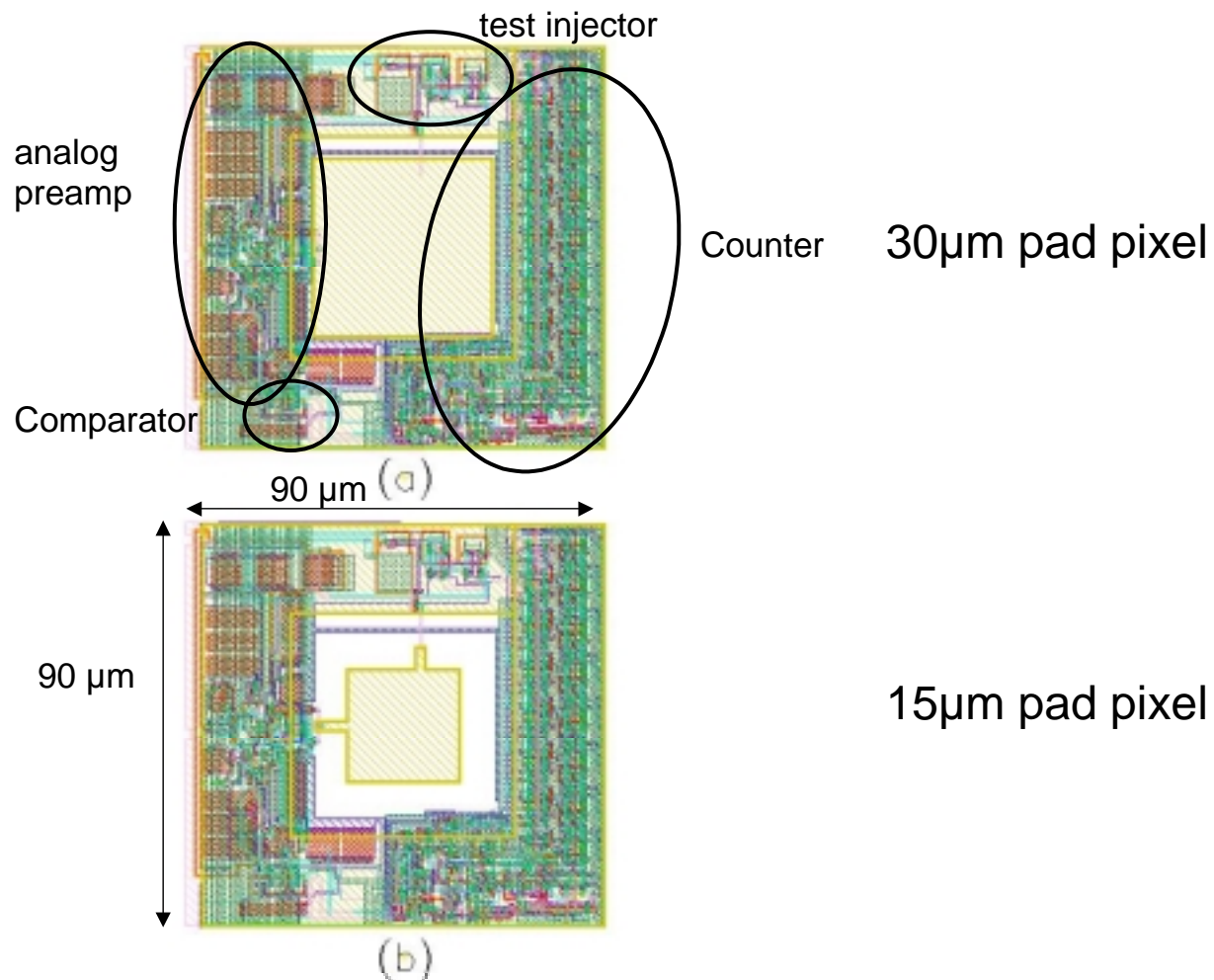
Half of the matrix with large input pads



ASIC layout



Pixels layout



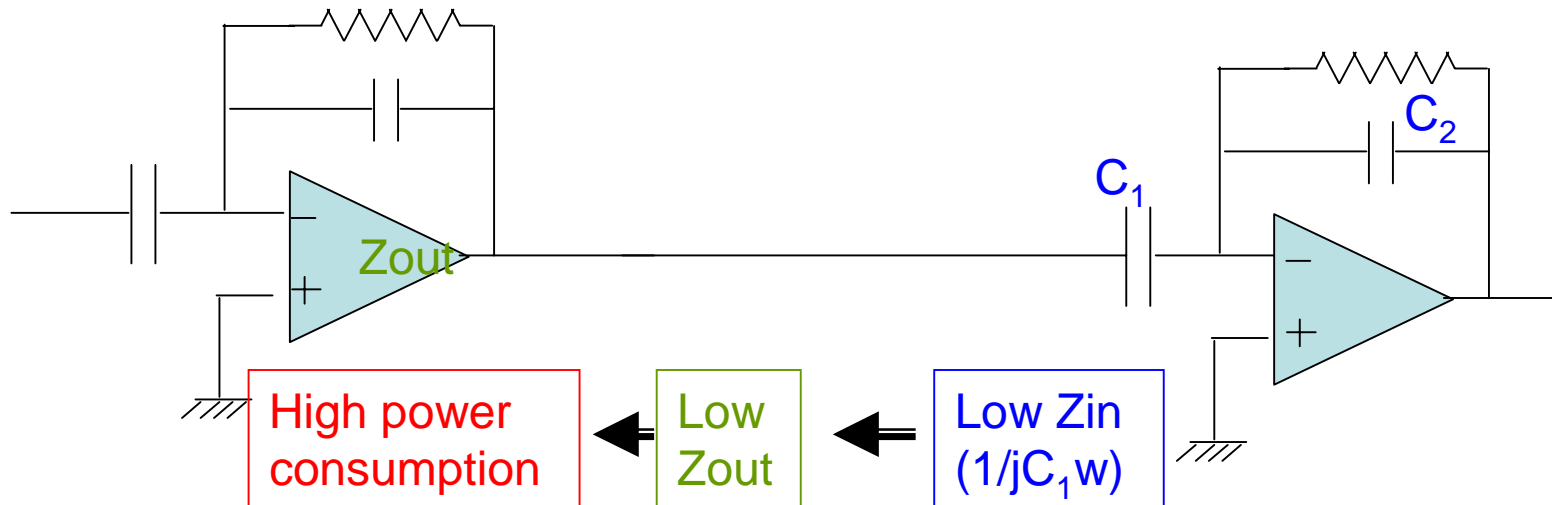
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Objectives are the same as for almost all counting ASICs, i.e. :

- high counting rate,
- high sensitivity,
- low power consumption.

Initial analysis : standard preamplifier schematics

The basic objective was to overpass the power consumption limitation of standard preamplifier schematics.



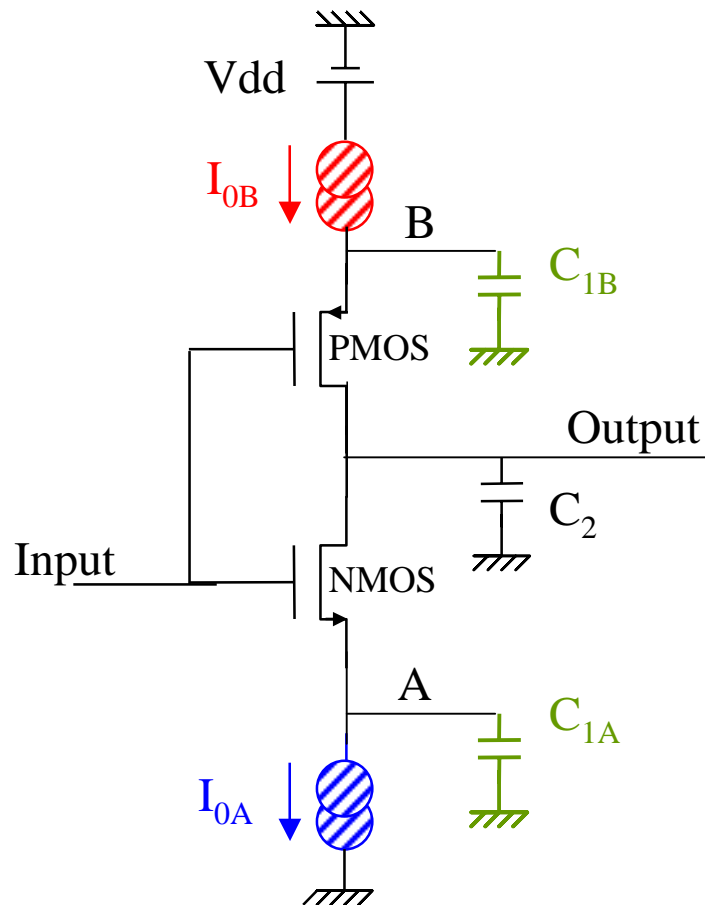
Problem :

Gain is defined by $-C_1/C_2$

Thus high gain requires high C_1 , thus low input impedance ($1/jC_1\omega$).

Thus, if stages are to be cascaded, previous stage has to have a low output impedance, and then has a high power consumption.

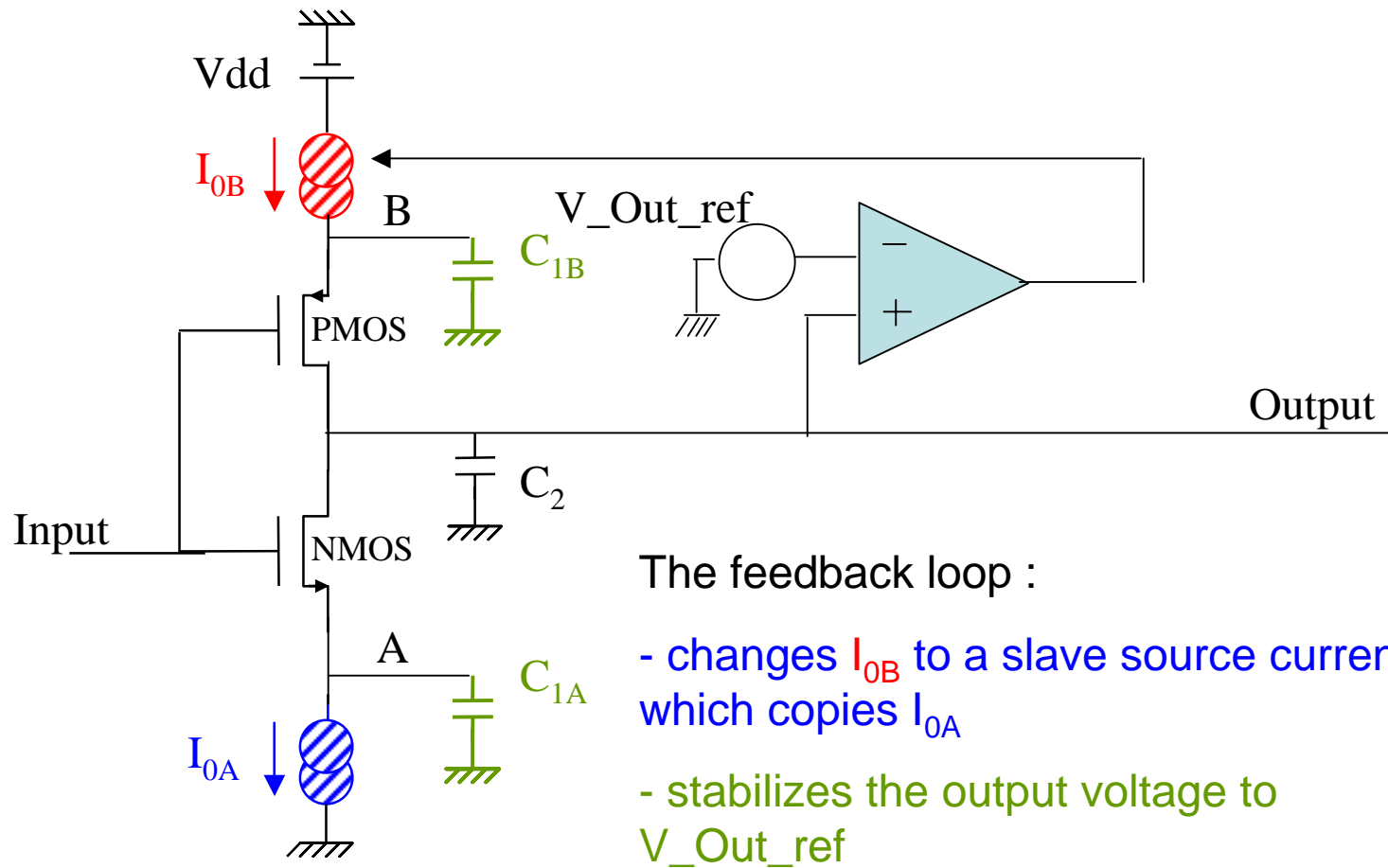
Preamplifier basic ideas : DC state



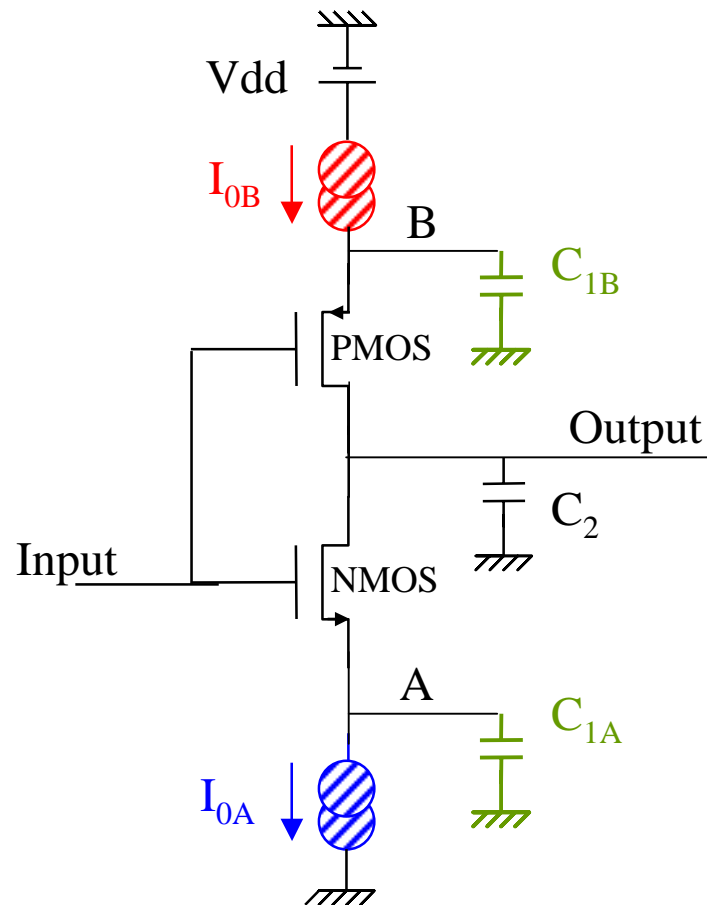
Use 2 current sources, I_{0A} and I_{0B} , with $I_{0A} = I_{0B}$.

But it is of course practically impossible to get 2 identical current sources on a circuit, so the final schematics will be...

Preamplifier basic ideas : DC state



Preamplifier basic ideas : DC state

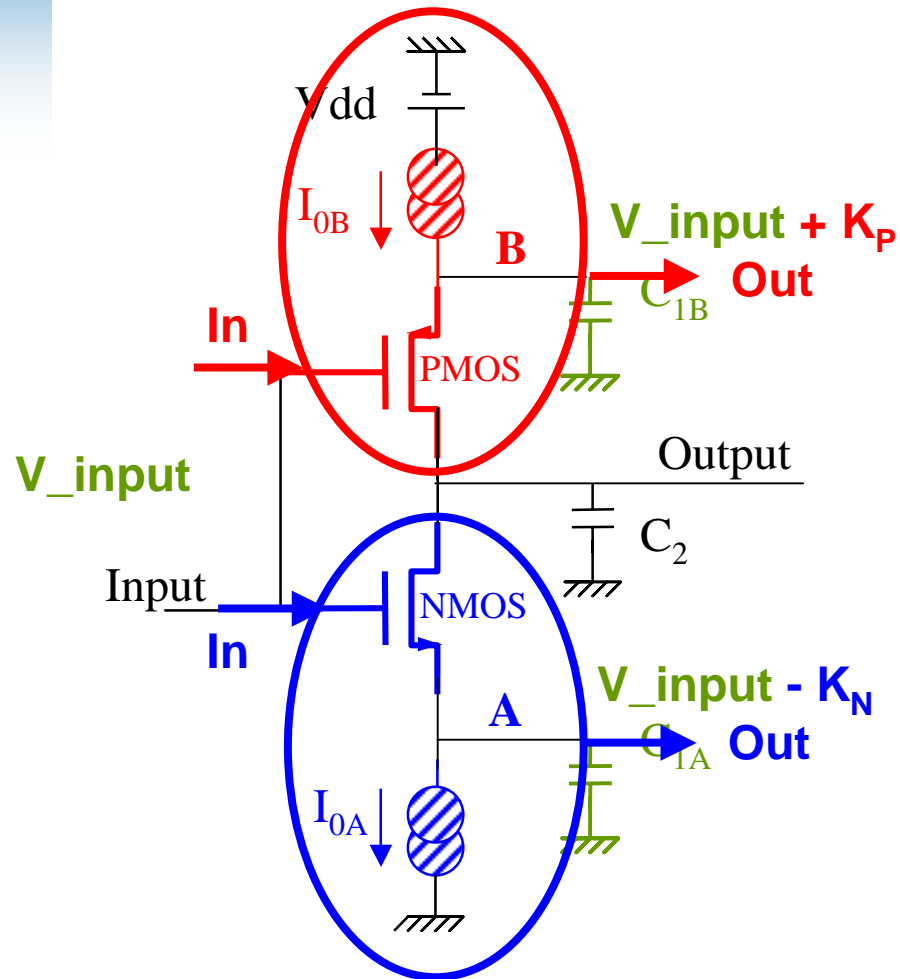


To explain the schematics behavior,
let us come back to the basic idea with

$$I_{0A} = I_{0B}$$

and V_{output} stabilized to $V_{\text{out-ref}}$

Preamplifier basic ideas : DC state



One way to explain the DC state is to recognize in the schematics, 2 following amplifiers :

a NMOS following amplifier

And then,

$$V_A = V_{\text{input}} - K_N$$

with K_N a constant value depending on the NMOS threshold voltage V_{TN} and on I_{0A}

and

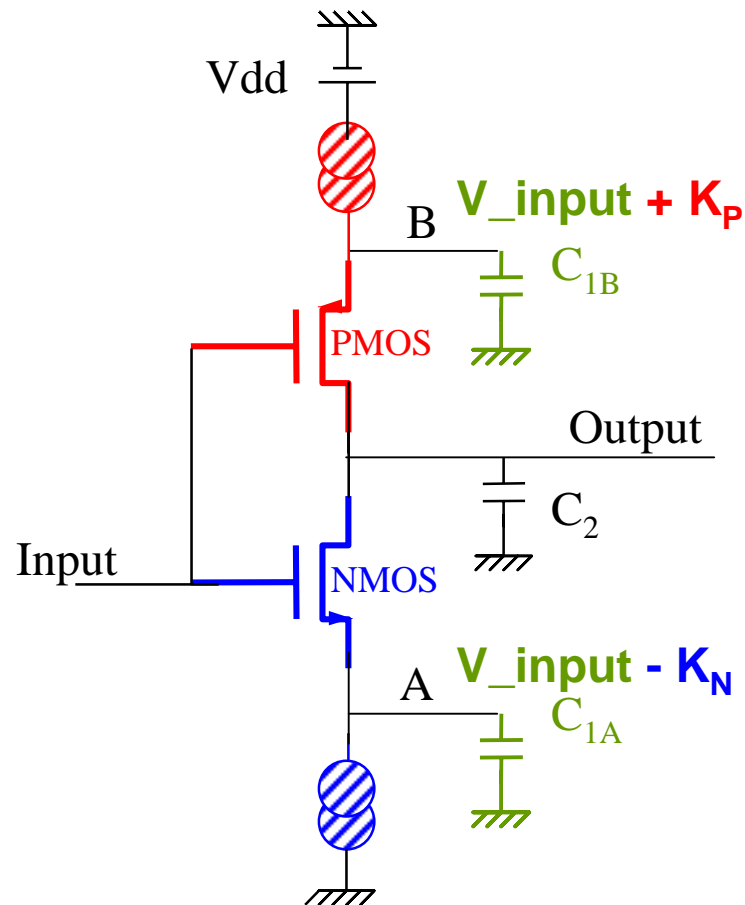
a PMOS following amplifier

And then,

$$V_B = V_{\text{input}} + K_p$$

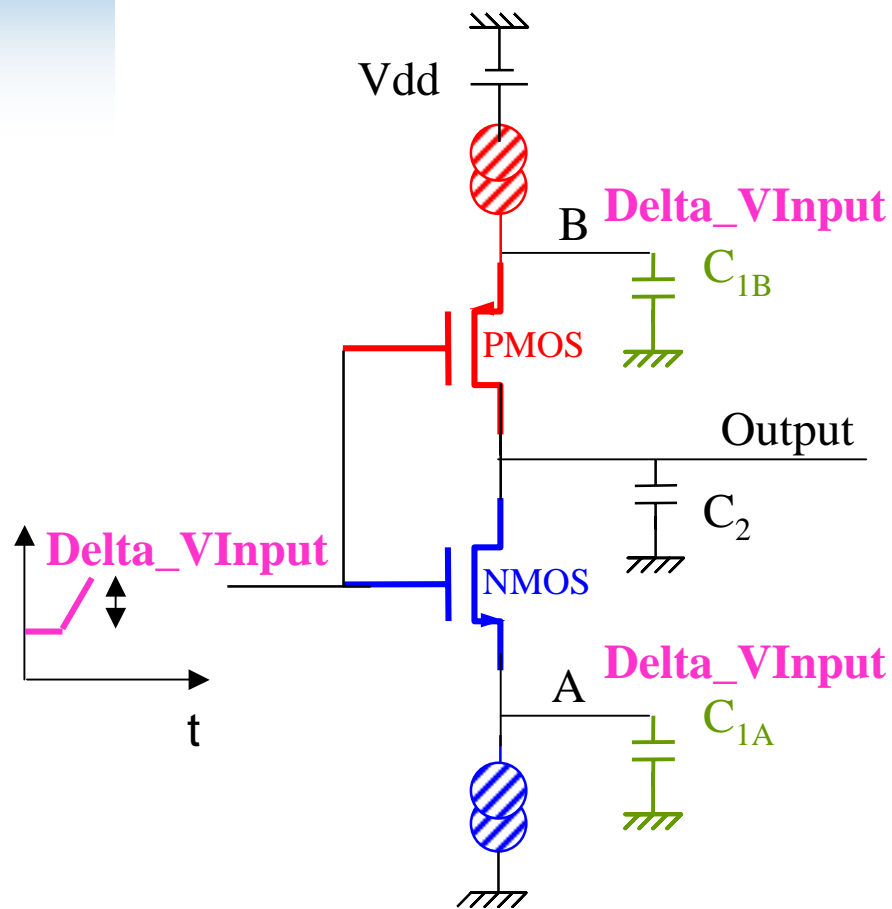
with K_p a constant value depending on the PMOS threshold voltage V_{TP} and on I_{0B}

Preamplifier basic ideas : dynamic behavior



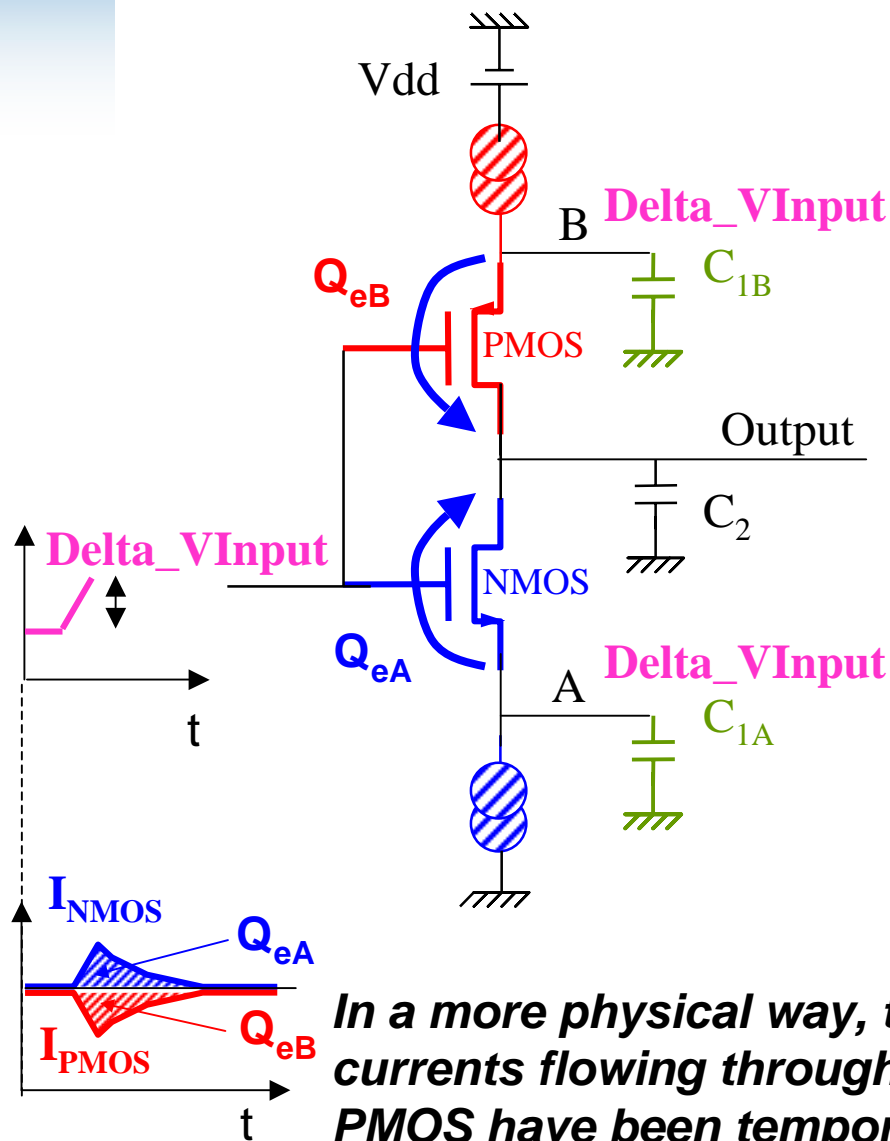
Let us now look to the dynamic behavior.

Preamplifier basic ideas : dynamic behavior



If V_{input} is increased by ΔV_{input} ,
Then V_A and V_B also increase by ΔV_{input} (due to the 2 previously identified following amplifiers).

Preamplifier basic ideas : dynamic behavior



If V_{input} is increased by ΔV_{input} ,
Then V_A and V_B also increase by ΔV_{input} .

V_A increases :

This means that a negative charge (electrons) Q_{eA} leaves from C_{1A} to C_2 , through the NMOS.

$$Q_{eA} = - C_{1A} \times \Delta V_{input}$$

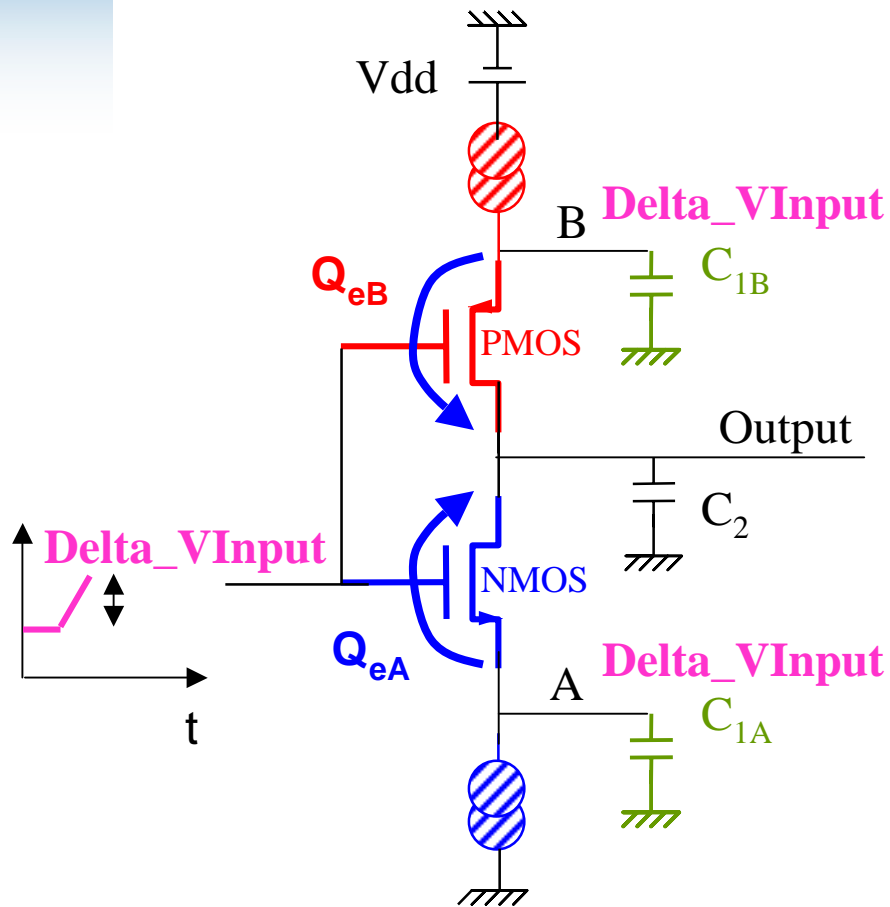
V_B increases :

This also means that a negative charge Q_{eB} leaves from C_{1B} to C_2 , through the PMOS.

$$Q_{eB} = - C_{1B} \times \Delta V_{input}$$

In a more physical way, this means that DC currents flowing through the NMOS and the PMOS have been temporary modified.

Preamplifier basic ideas : dynamic behavior



Thus

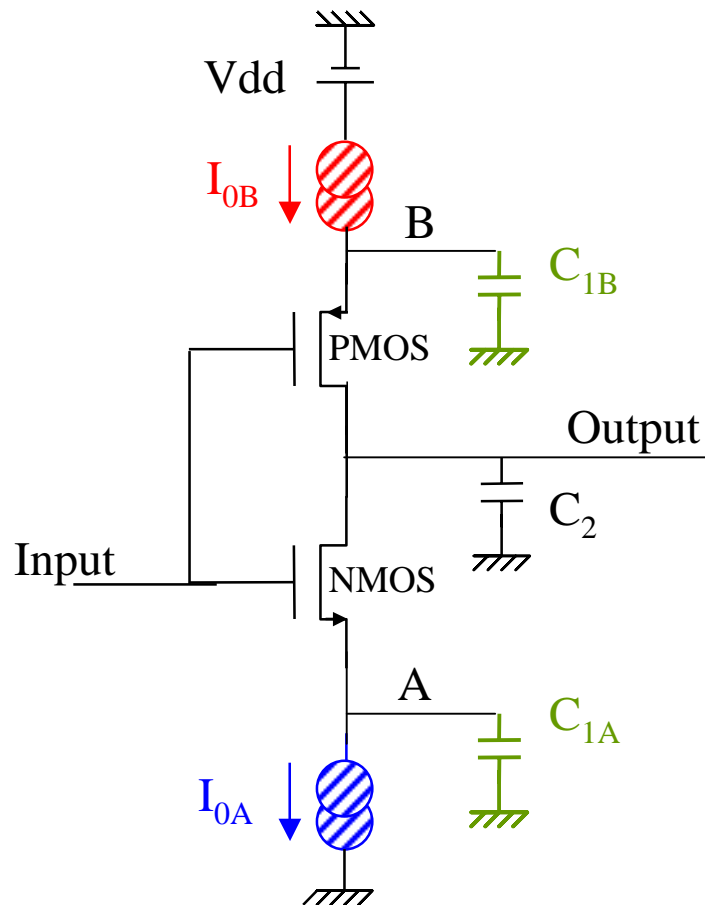
$$\Delta V_{Output} = (Q_{eA} + Q_{eB}) / C_2$$

$$= - (C_{1A} + C_{1B}) / C_2 \times \Delta V_{Input}$$

or

$$\text{Gain} = - (C_{1A} + C_{1B}) / C_2$$

Preamplifier basic ideas



Conclusions :

$$\text{Gain} = - (C_{1A} + C_{1B}) / C_2$$

Static gain is defined by a ratio of capacitors,

It is independent upon the input preamplifier capacitance

Power consumption separately defines the preamplifier bandwidth

Current is reused, in the NMOS the PMOS, thus limiting the power consumption for a targeted gain.

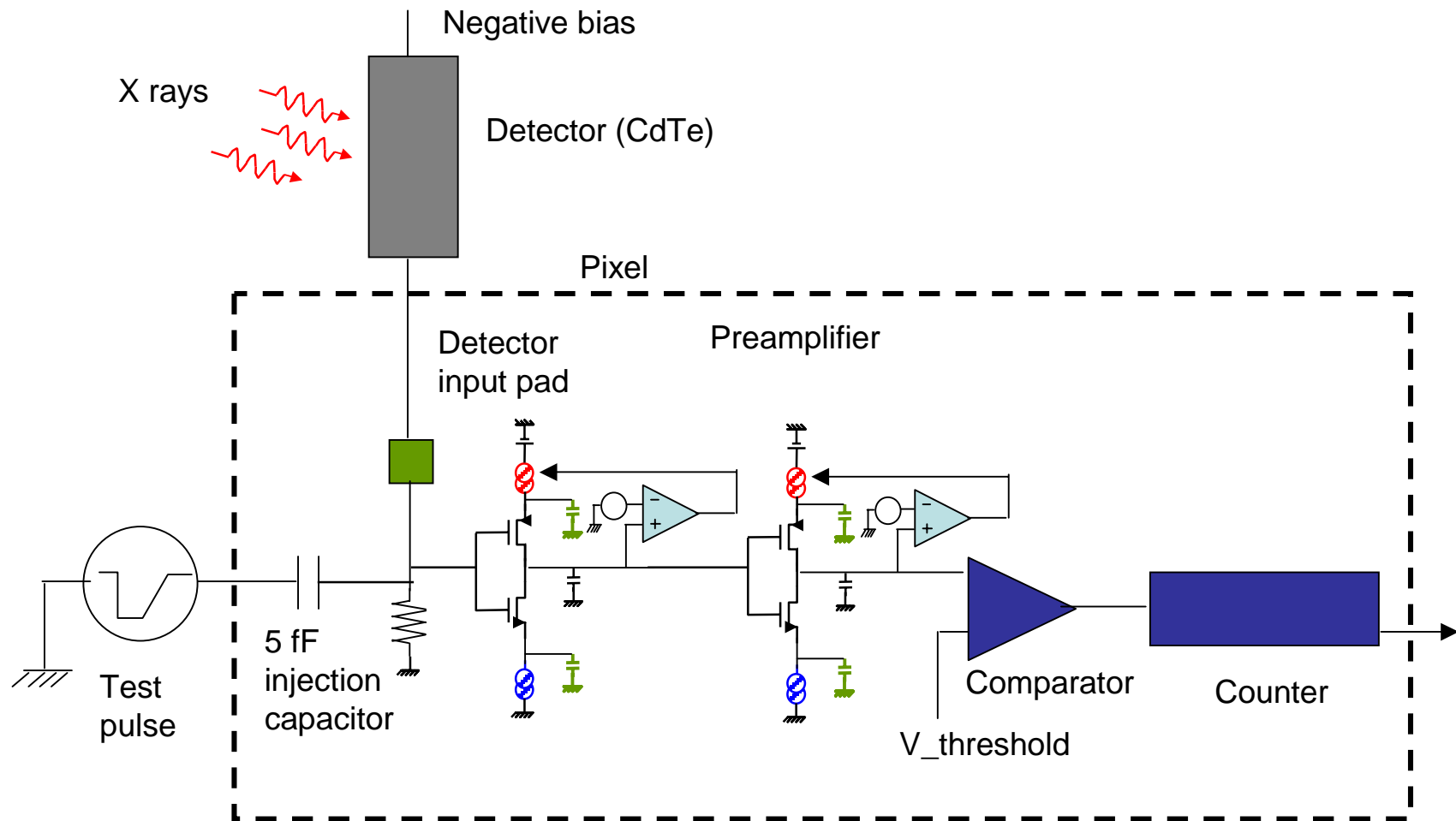
DC input value has no influence on the charge transfer. So, this stage is very tolerant to input voltage offsets

NB : this stage cannot deliver permanent current. It has to be connected to a high impedance input stage, but this is no problem with CMOS technology.

Final pixel schematics

The final pixel schematics is composed of :

- a current-voltage converter (a MOSFET acting as a resistor)
- 2 voltage-voltage previous amplifiers



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Electrical test results

All following results correspond to a
total pixel analog power consumption of

$$1400 \text{ nA} \times 3.3\text{V} = 4.6 \text{ }\mu\text{W}$$

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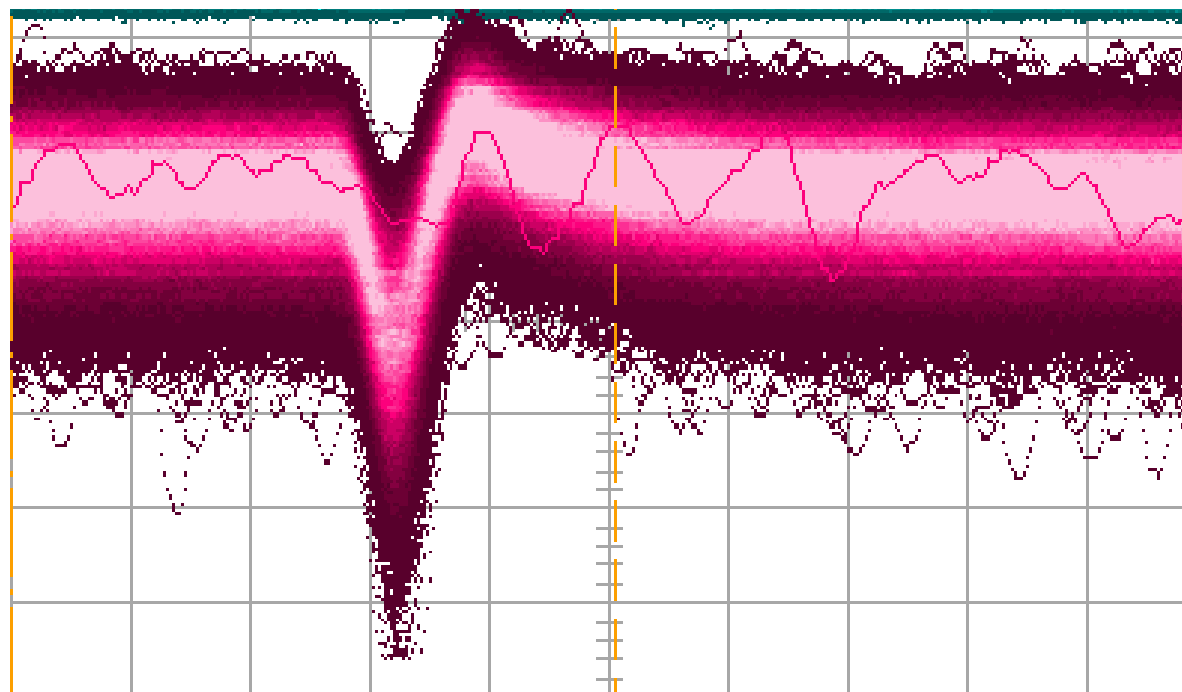
- - electrical test results
 - analog sensitivity
 - counting performance versus stimuli intensity
 - noise
 - counting performance versus stimuli Δt
 - electrical images

- future work
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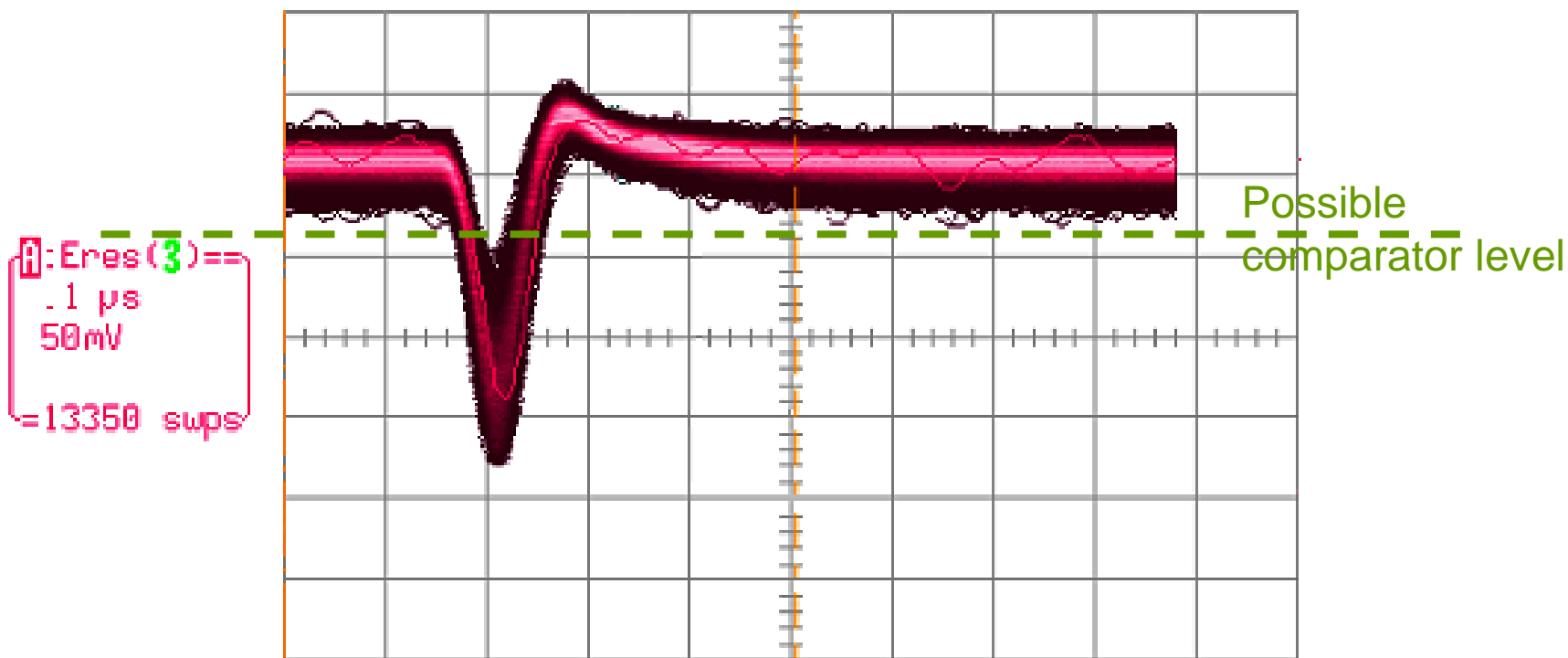
Sensitivity

500 electrons test injection is visible on the scope, but signal / noise is not good enough for counting

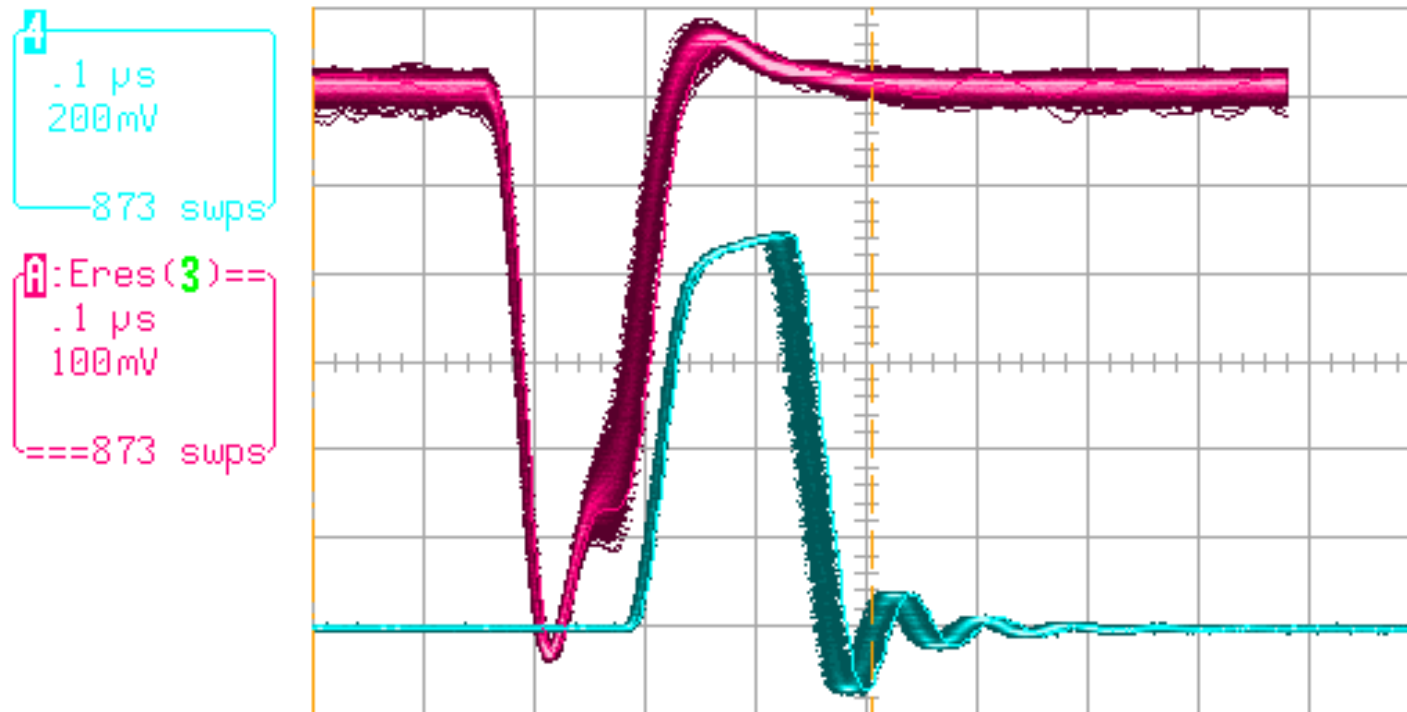
a:Eres(3) ==
 .1 μ s
 15.0mV
 =10114 swps



1200 electrons test injection is good enough for counting



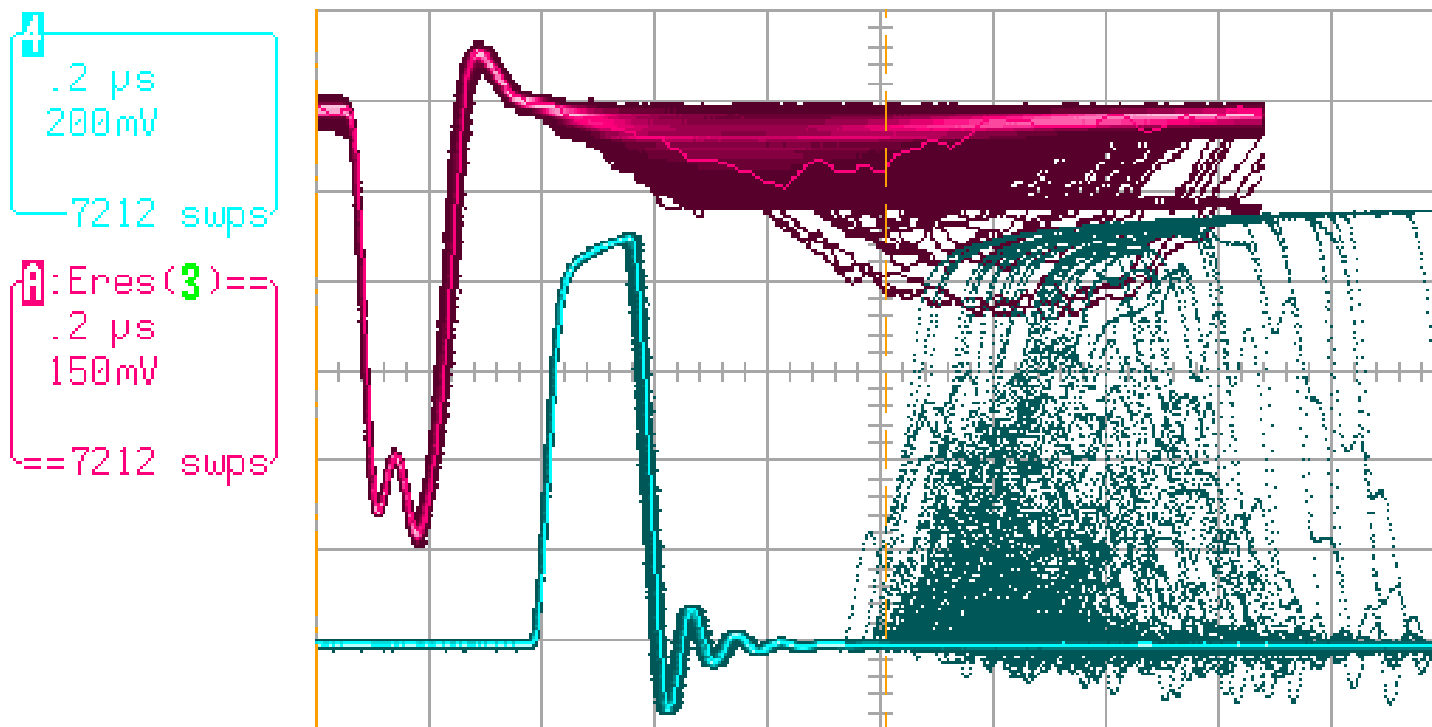
5000 electrons test injection is very easy to count



NB : Digital output is delayed on the scope display, to improve visibility

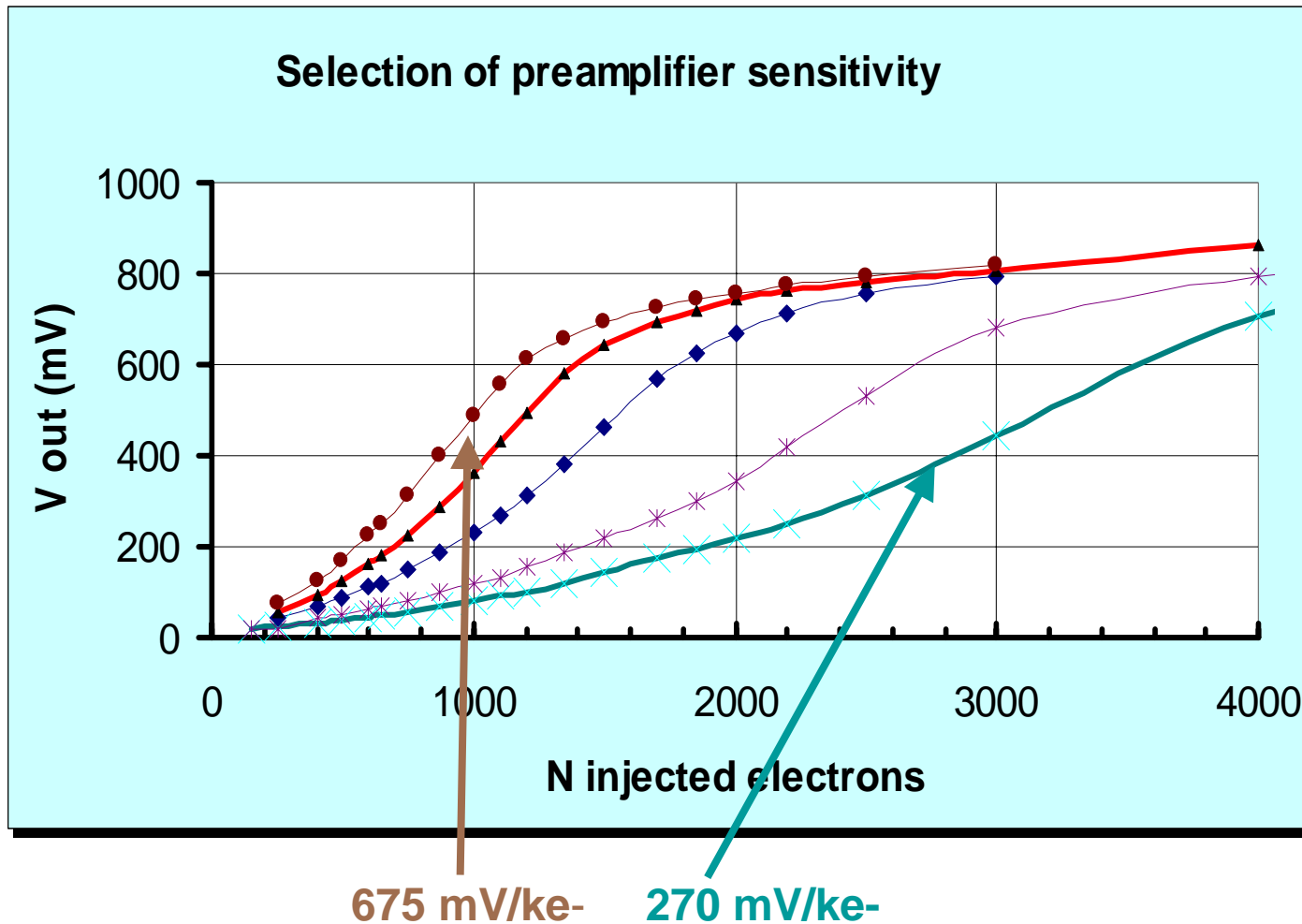
Sensitivity

10 000 electrons test injection creates an overshoot.
Not acceptable.



Sensitivity is very high and tunable

Adjusting feed back loop biasing, improves and **tunes the sensitivity**.

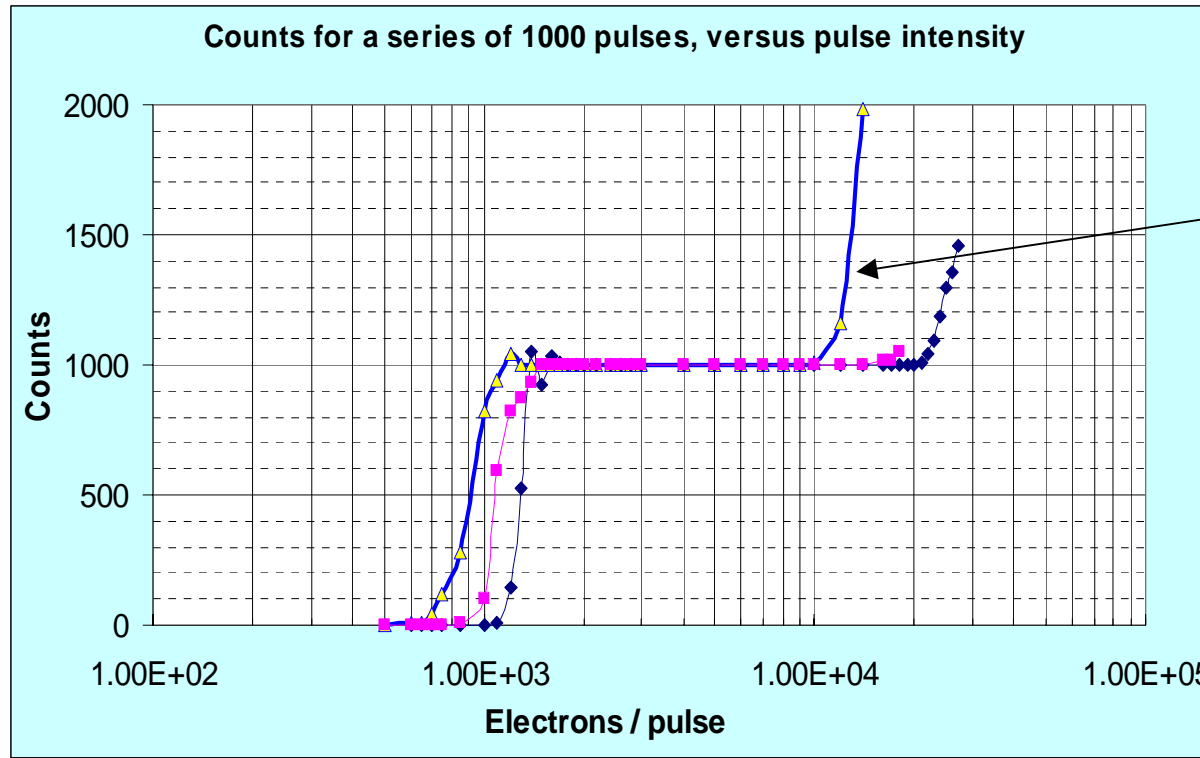


Outlook of the talk

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Counting a series of 1000 test pulses versus pulses intensity

Results for different feed back loop biasing



Circuit behavior is good over 1 decade variation of the input pulse

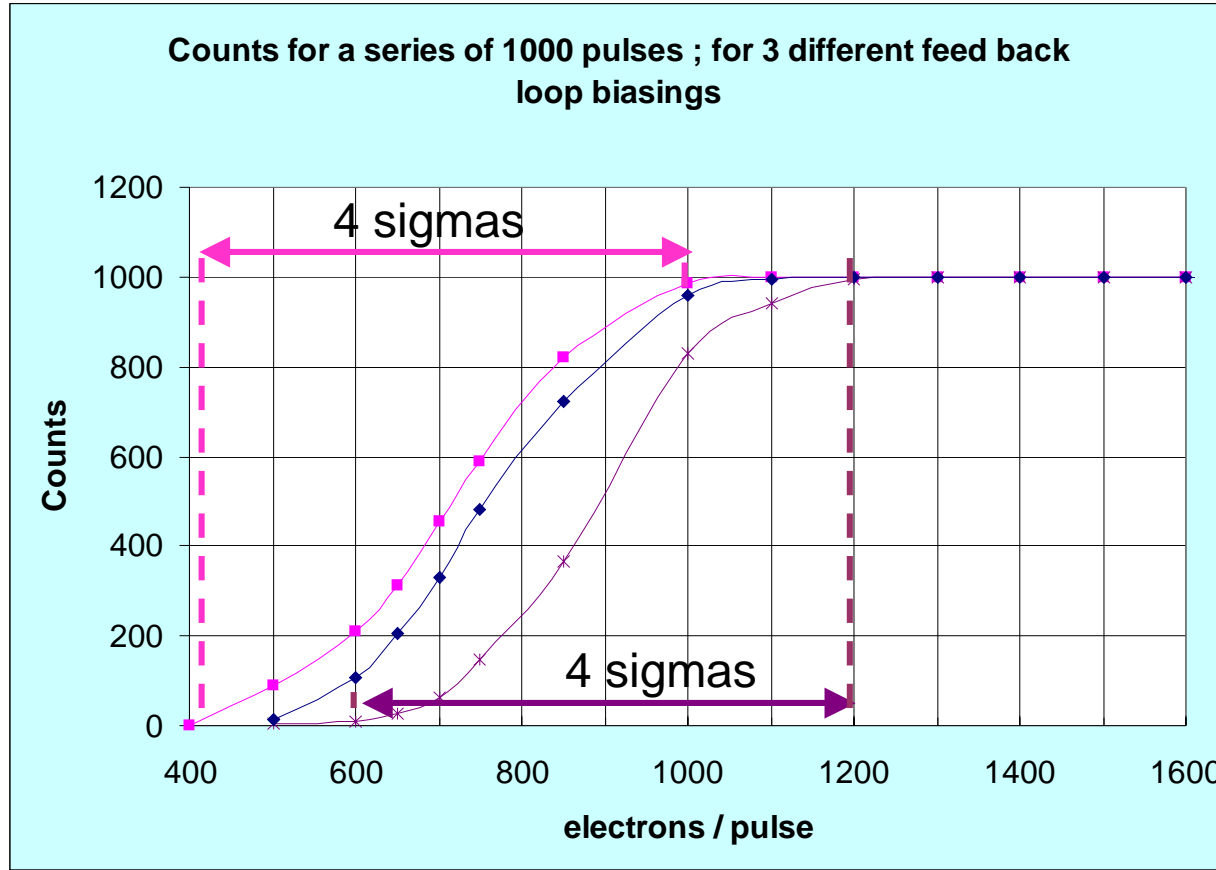
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Noise

Noise can be derived from the S curve.

Charge difference between 2.5% and 97.5% counts is 4 sigmas



rms noise = 150 electrons

Not dependent upon the feedback loop biasing

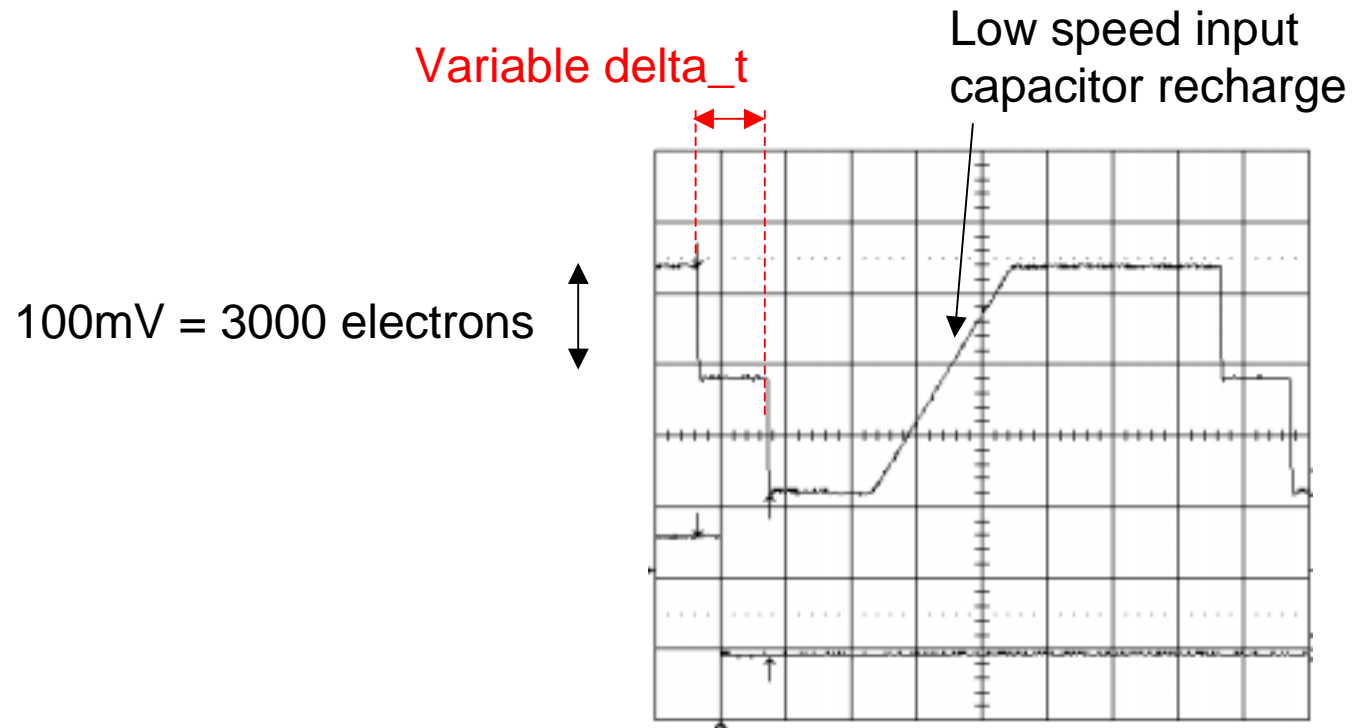
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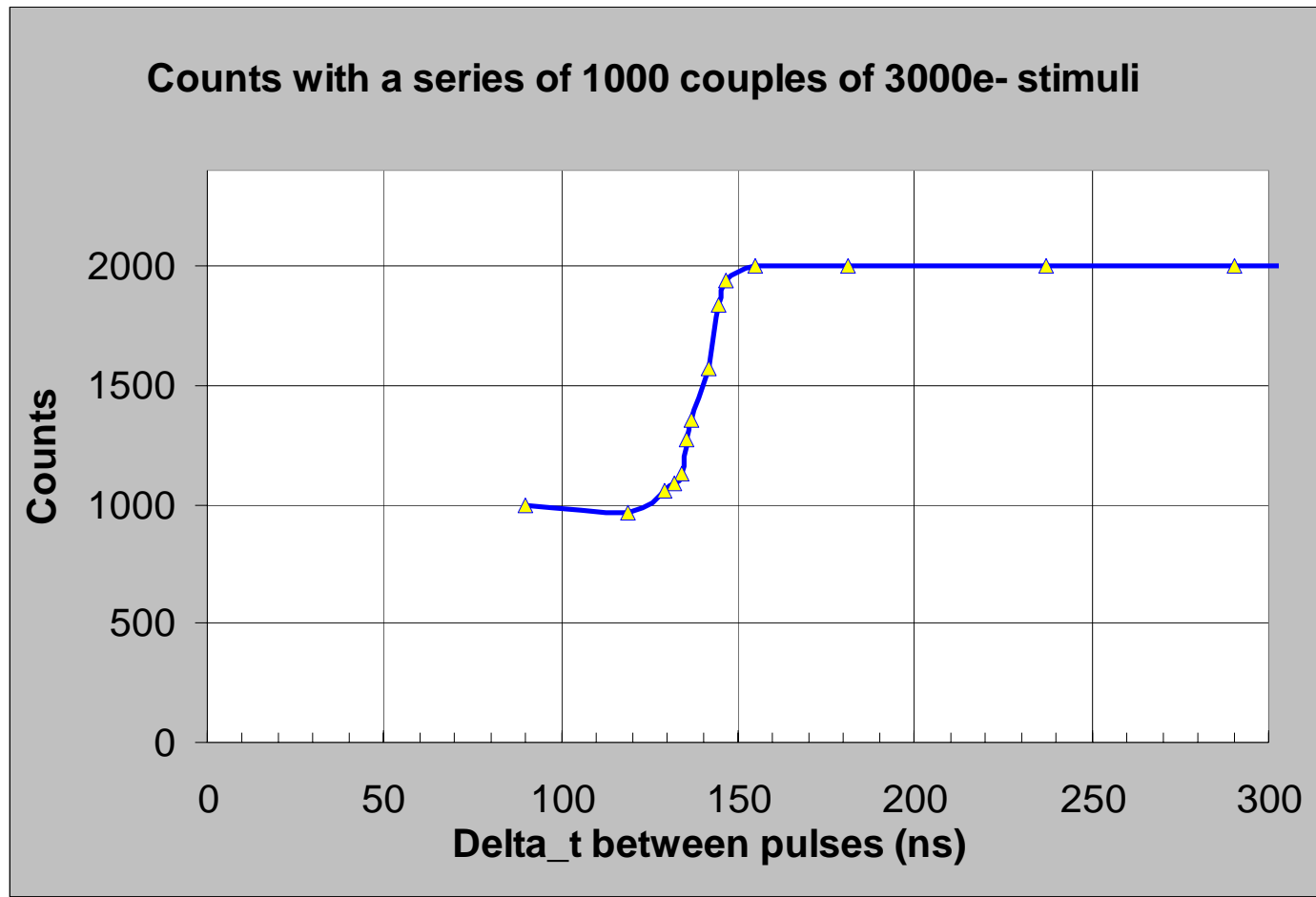
Counting versus stimuli delta_t



1000 couples of 3000 electron pulses were injected through the 5 fF input capacitor.

Delta_t was varied

Counting versus stimuli delta_t



3000 electron pulses distant by more than **150ns** are correctly counted

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- - electrical images

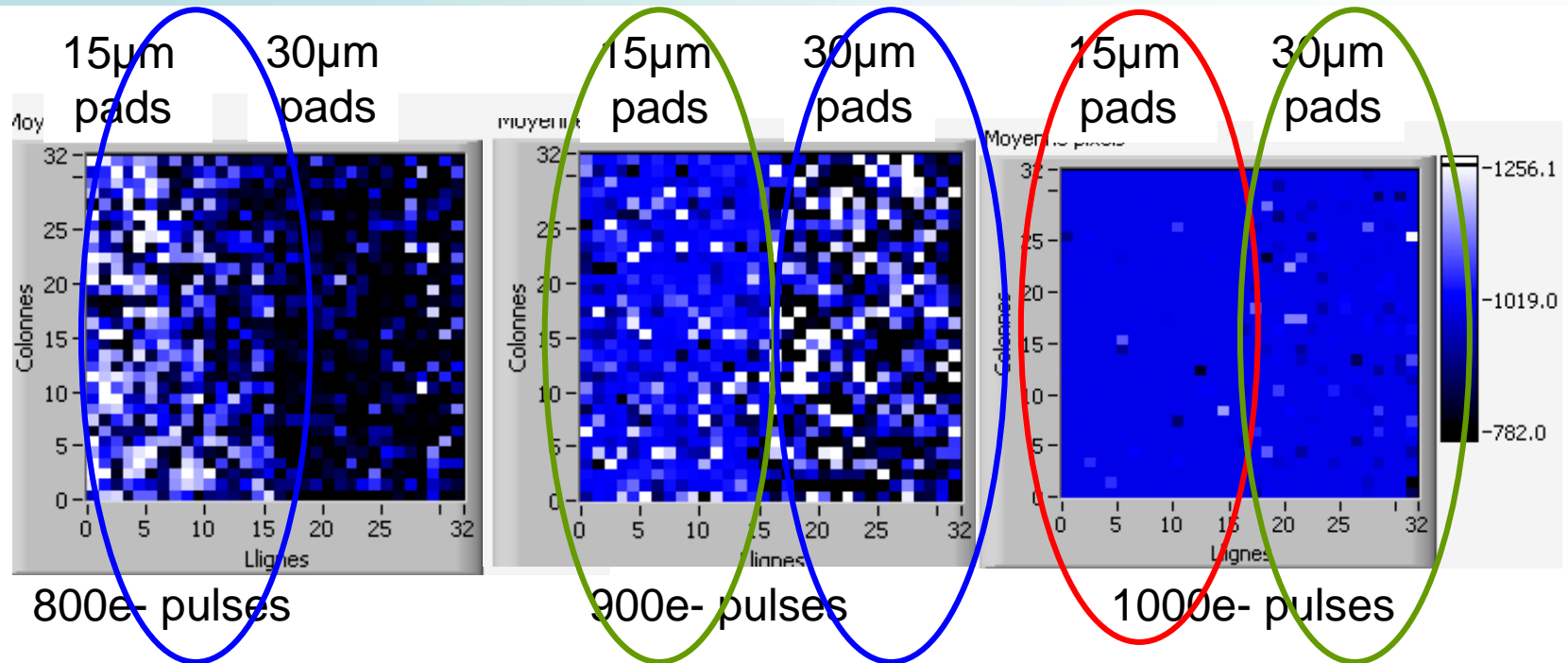
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Electrical images were obtained injecting a series of 1000 pulses, simultaneously on all the pixels.

Pulses intensity was varied.

Electrical images

Series of 1000 pulses on all the pixels



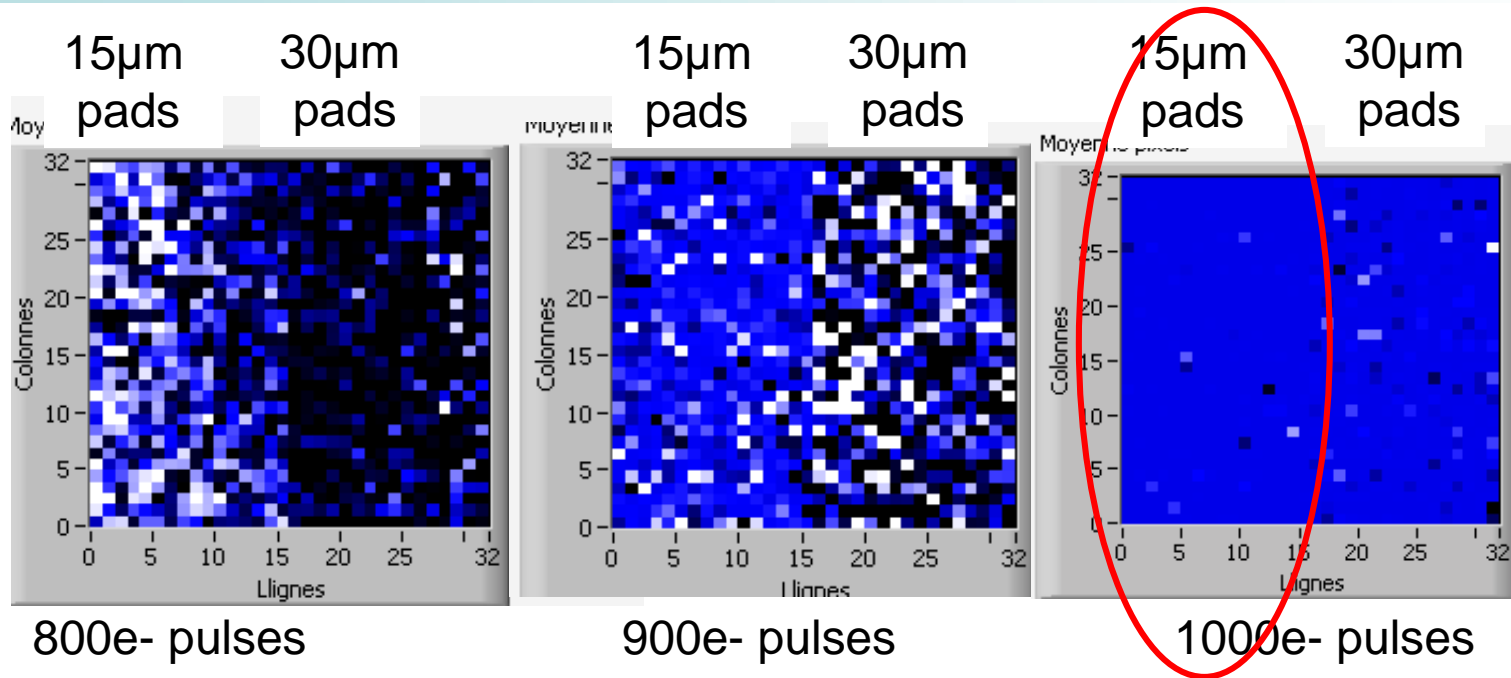
1000 electron pulses are almost perfectly counted with 15µm input pads

30µm input pads degrade the performance. About 100 electrons more are required to get the same performance.

Performance is expected to degrade by a few hundred electrons when the ASIC is coupled to a detector

Electrical images

Series of 1000 pulses on all the pixels



Analog sensitivity is high enough to overpass comparators threshold variations.

An homogeneous image is obtained, without requiring pixel threshold adjustment.

- ASIC objectives and global schematics
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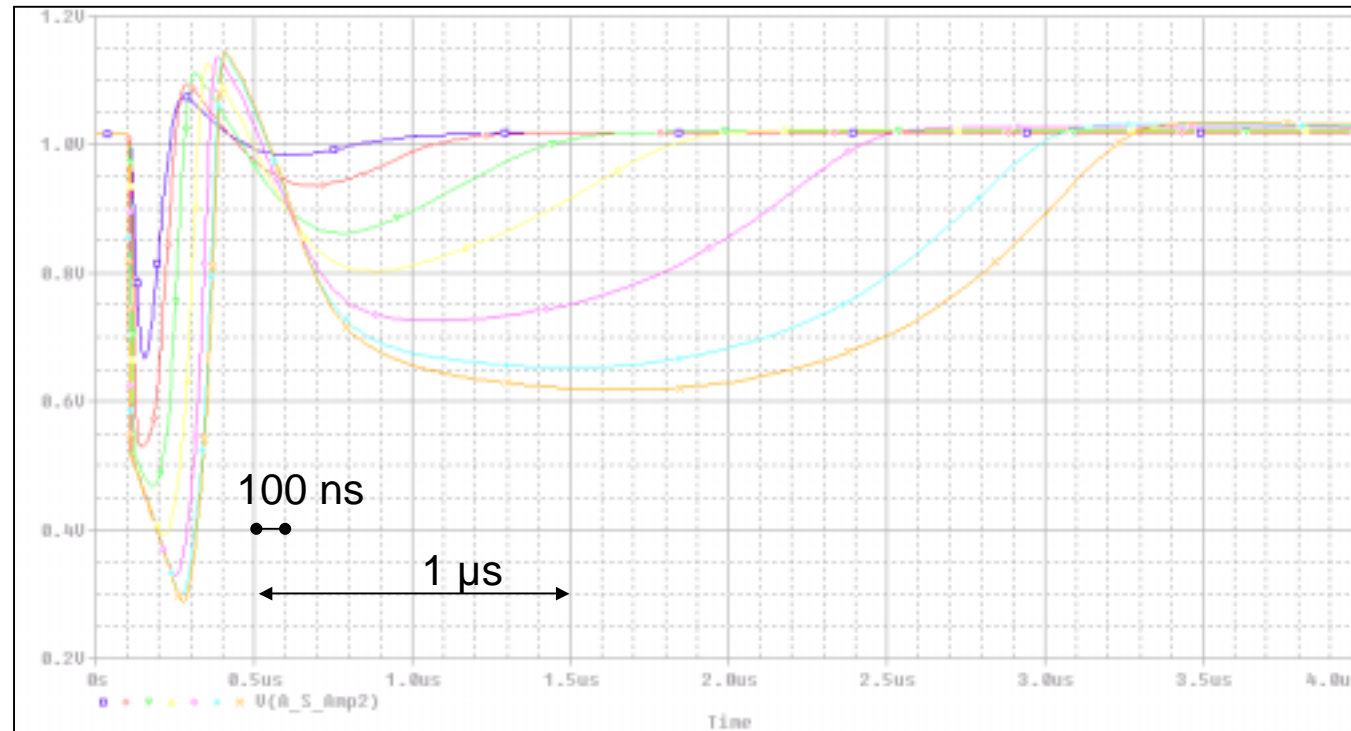
Future work

1- The ASIC will be more deeply studied : in particular behavior at other power consumptions will be looked at

2- The ASIC will be coupled to photodetectors (namely CdTe or CdZnTe)

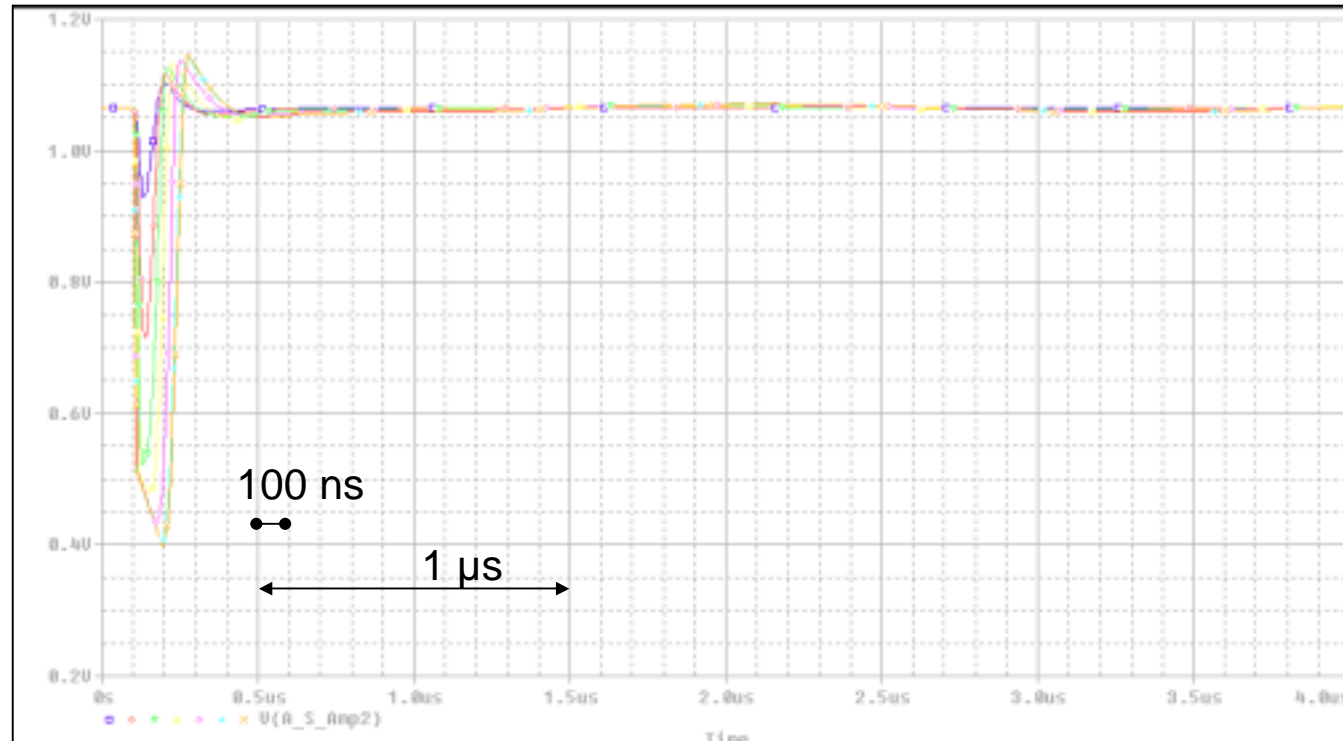
3- A redesign will be done.
In particular the overshoot for large input pulses will be cancelled

Present ASIC overshoot simulation



Simulated analog output for input pulses of
500 ; 1000 ; 2000 ; 4000 ; 8000 ; 16000 ; 32000 electrons

Next ASIC overshoot simulation



Simulated analog output for input pulses of
500 ; 1000 ; 2000 ; 4000 ; 8000 ; 16000 ; 32000 electrons

Sensitivity is lower, but still high (300mV / ke-)
Overshoot and speed are greatly enhanced

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⇒ - Conclusions

Conclusions

A new preamplifier for X ray counting ASICs has been tested.

It gives :

Pixel power consumption	4.6 μ W
Tunable sensitivity	270 to 675 mV / ke-
Rms noise	150 e-
Input pulse dynamic range	1 000 to 10 000 e-
Minimum Δt @ 3000e- pulses	150 ns
Minimum image threshold	\approx 1 000 e-

In the next future, the ASIC will be coupled to a detector.

Next ASIC will increase the input pulses dynamic range.

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Thank you for attention

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