Moore's law and challenges for future pixel detector designs

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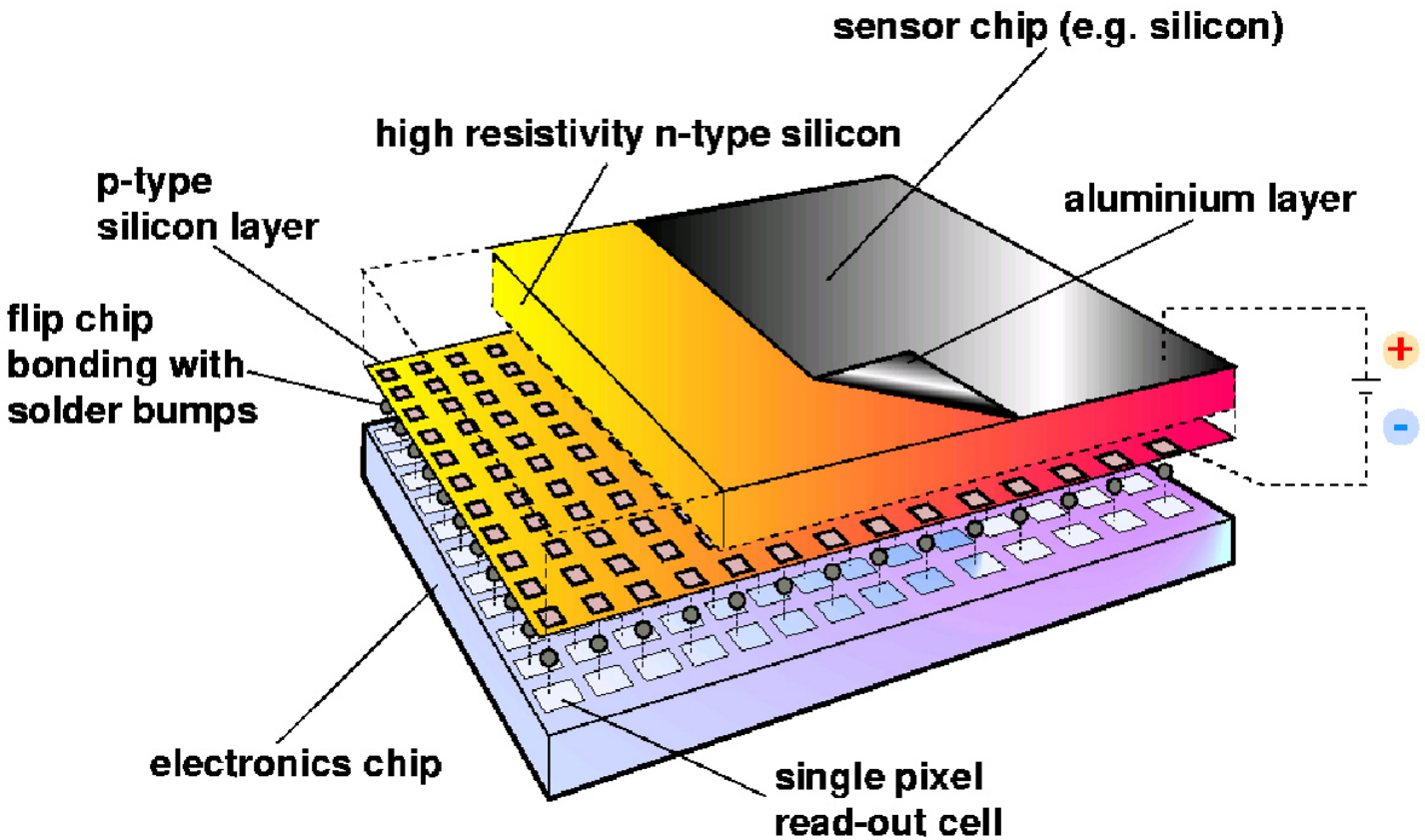
Outline

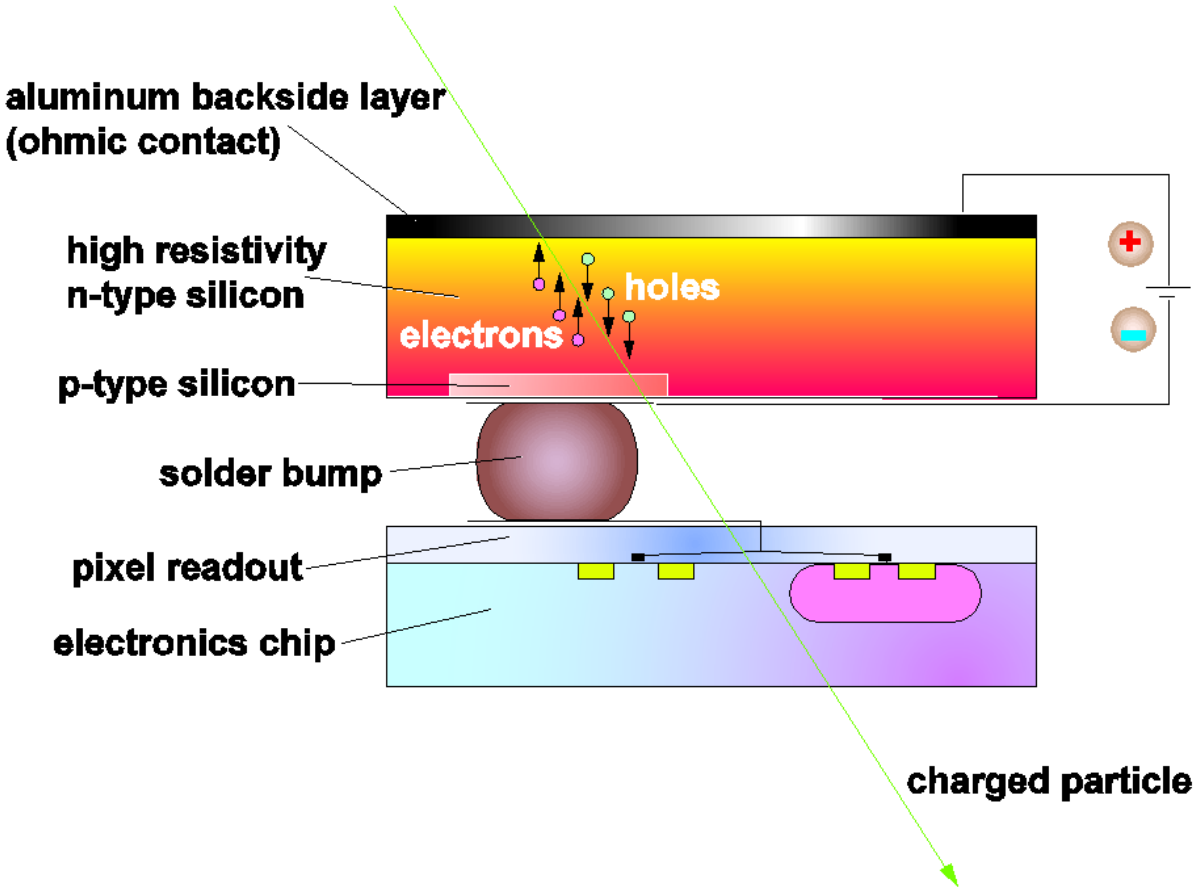
- Hybrid pixel detectors – basic concepts
- Moore's law and developments in CMOS
- Impact on pixel chip design
- Future trends in CMOS
- A present day pixel imaging system
- Other emerging technologies
- Conclusions

- A demonstration a portable radiation imaging detector

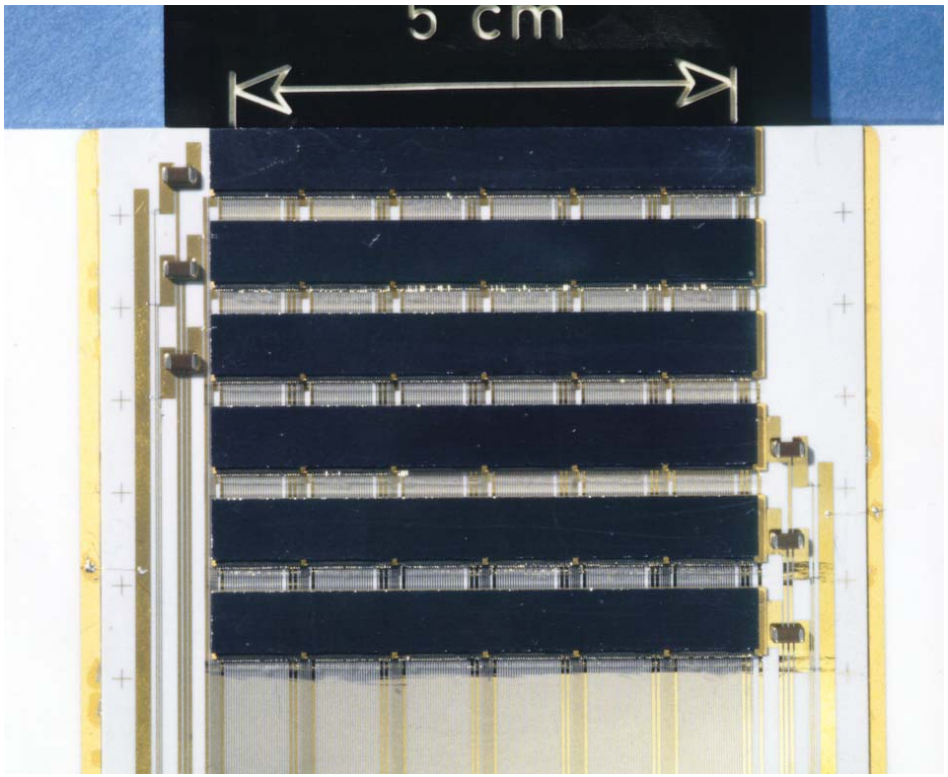
Hybrid Pixel Detector



Hybrid Pixel Detector - Cross Section



A (by now rather old) pixel detector array



36 000 pixels

6 ladders of 6 chips

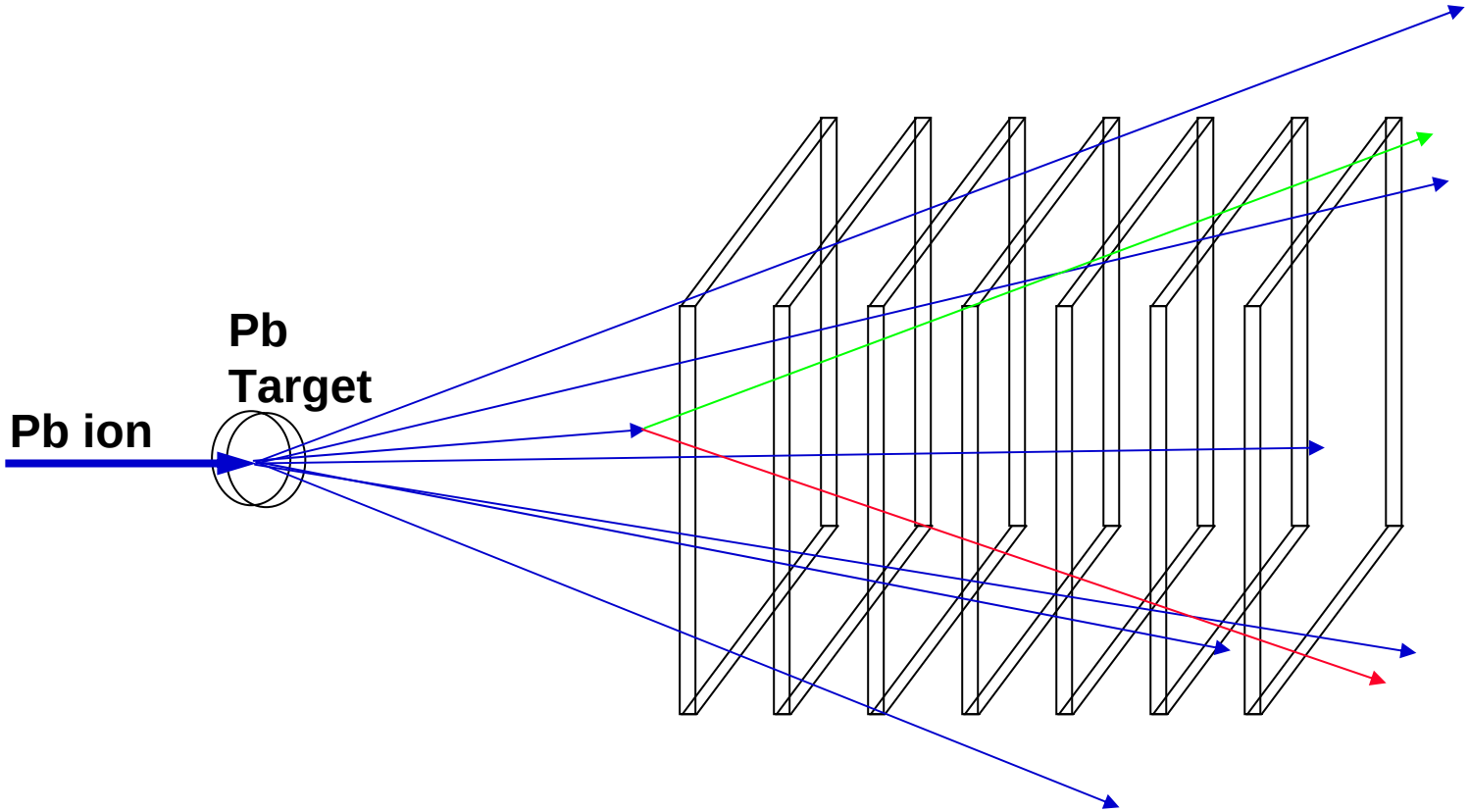
Each chip has 1000 pixels

2 arrays make up one logical plane

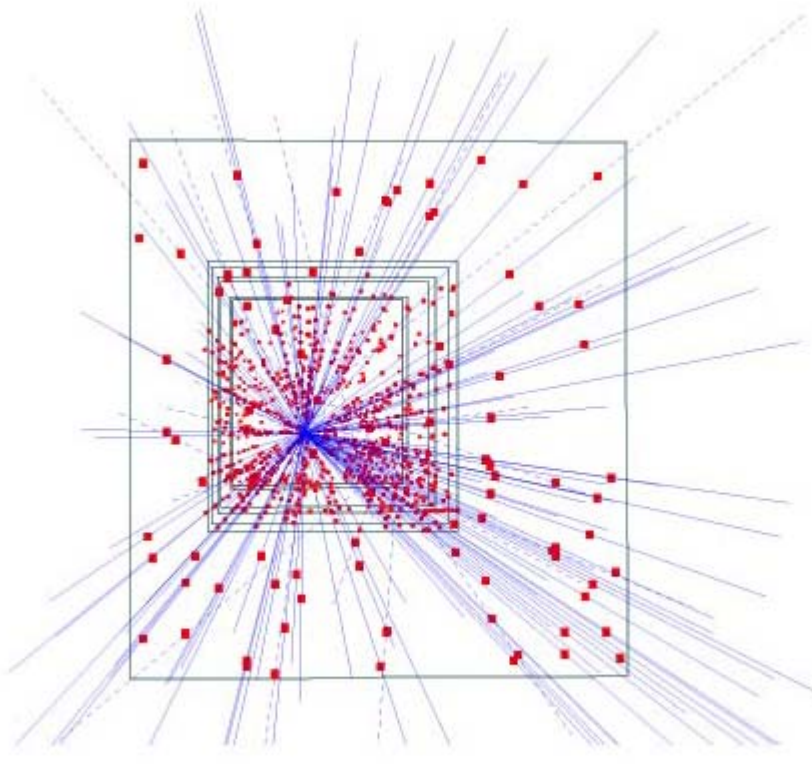
[E. Heijne, E. Chesi]

Work carried out by RD19 for WA97.

Hybrid pixel detector arrangement in a fixed target heavy ion experiment (CERN WA97)



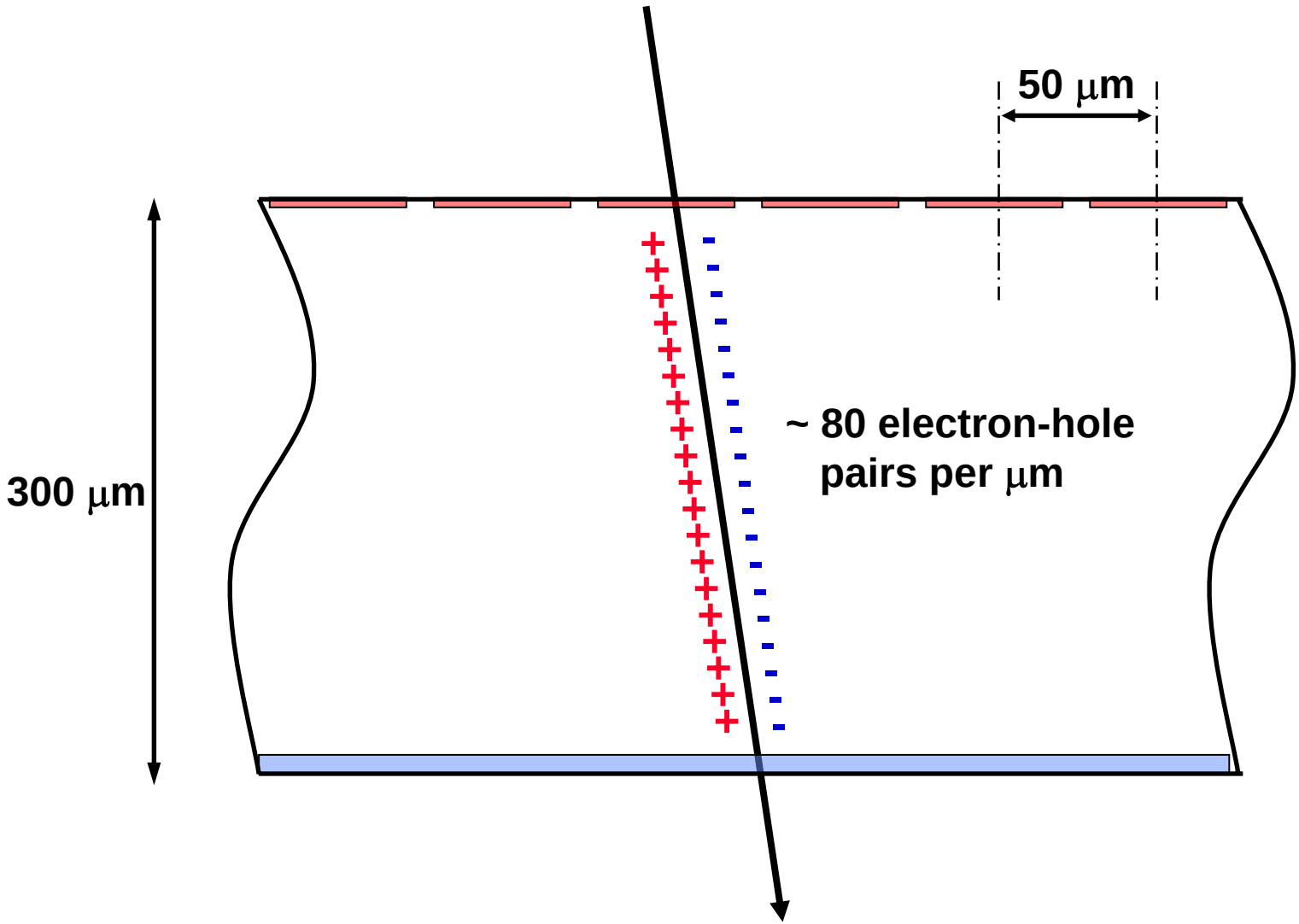
CERN Experiment WA97 (1995)



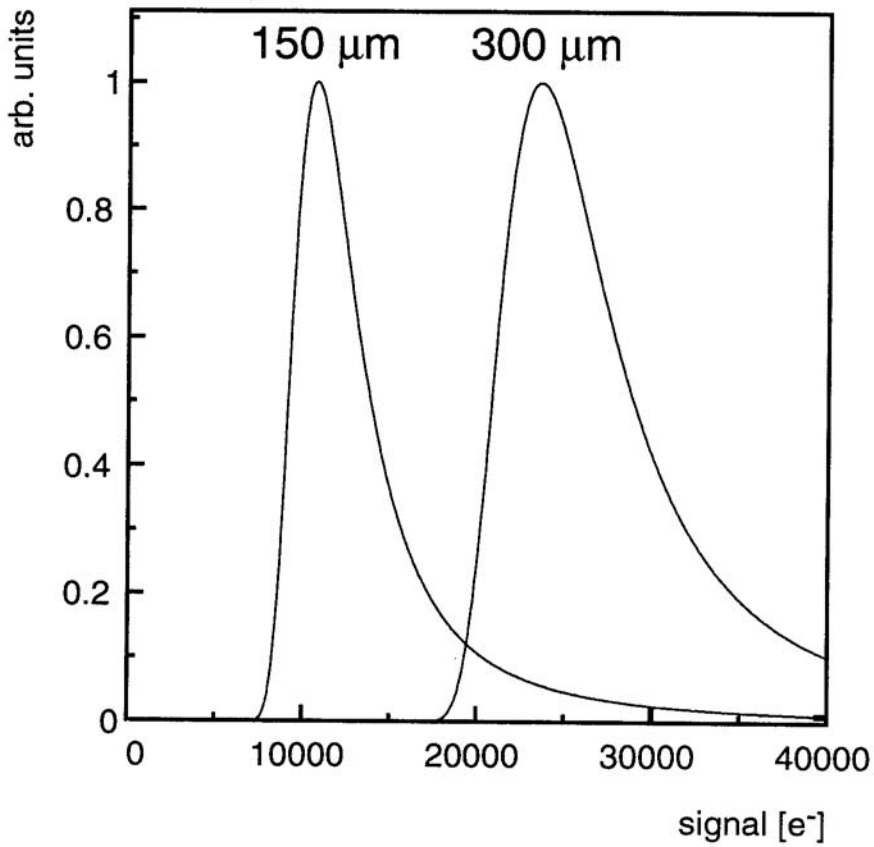
5 x 5 cm^2 area
7 detector planes
~ 0.5 M pixels
Pixel dimensions 75 x 500 μm^2
Trigger precision 1 μsec
1 kHz trigger rate

NO hits unassociated with particle tracks => WHY??

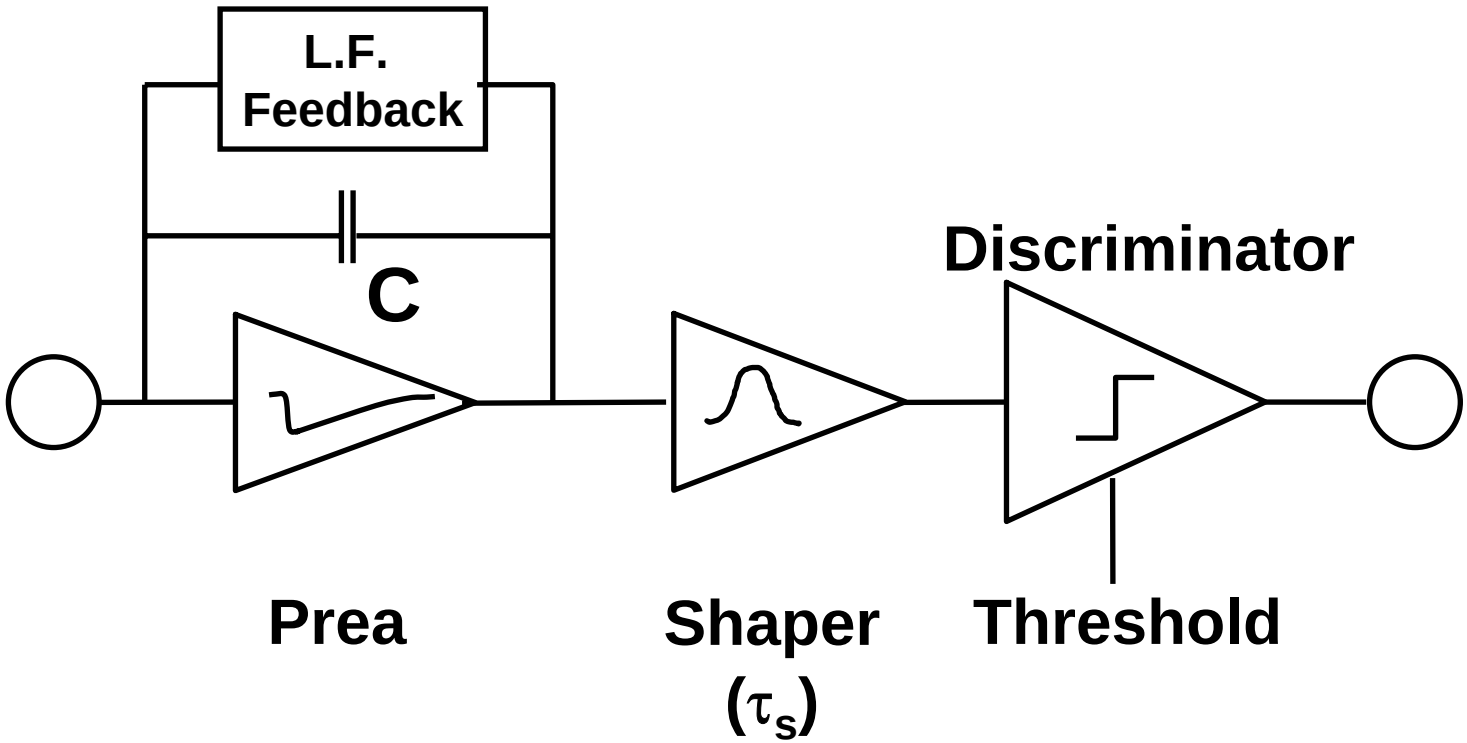
Minimum Ionizing Particle in Si Pixel Sensor



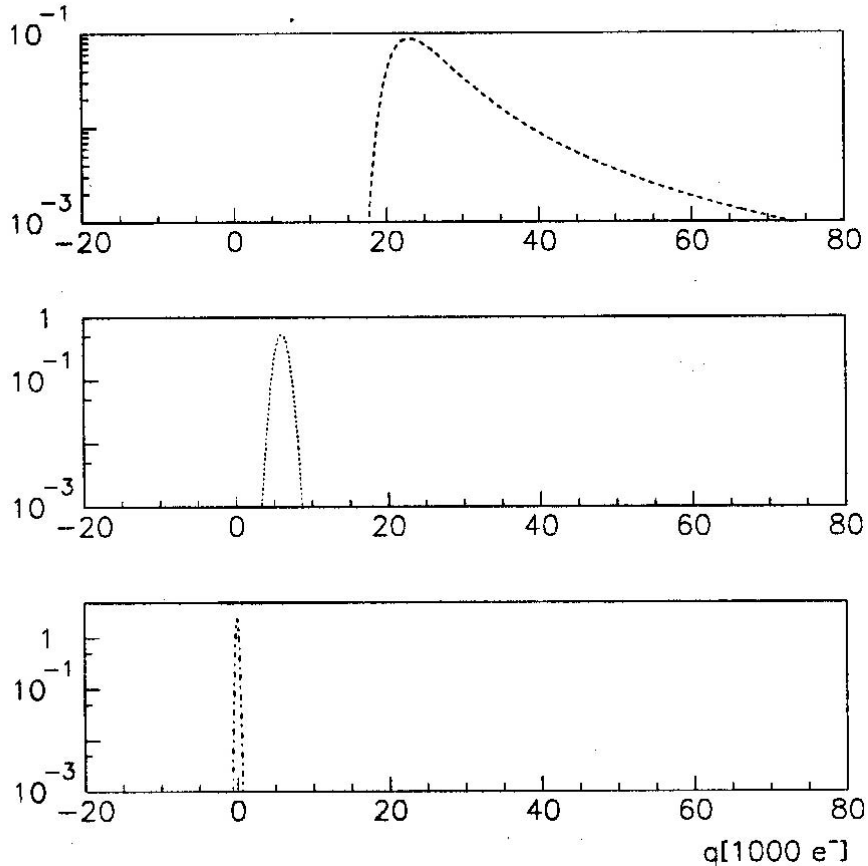
Minimum Ionizing Charge Deposition in Si



Typical Front-end for HEP Pixel



Signal, Threshold, Noise



Landau for 300 μm detector

Threshold and threshold variation

Noise

Because of charge sharing between pixels the threshold is normally set around 1/3rd Landau peak while maintaining optimum detection efficiency and spatial resolution

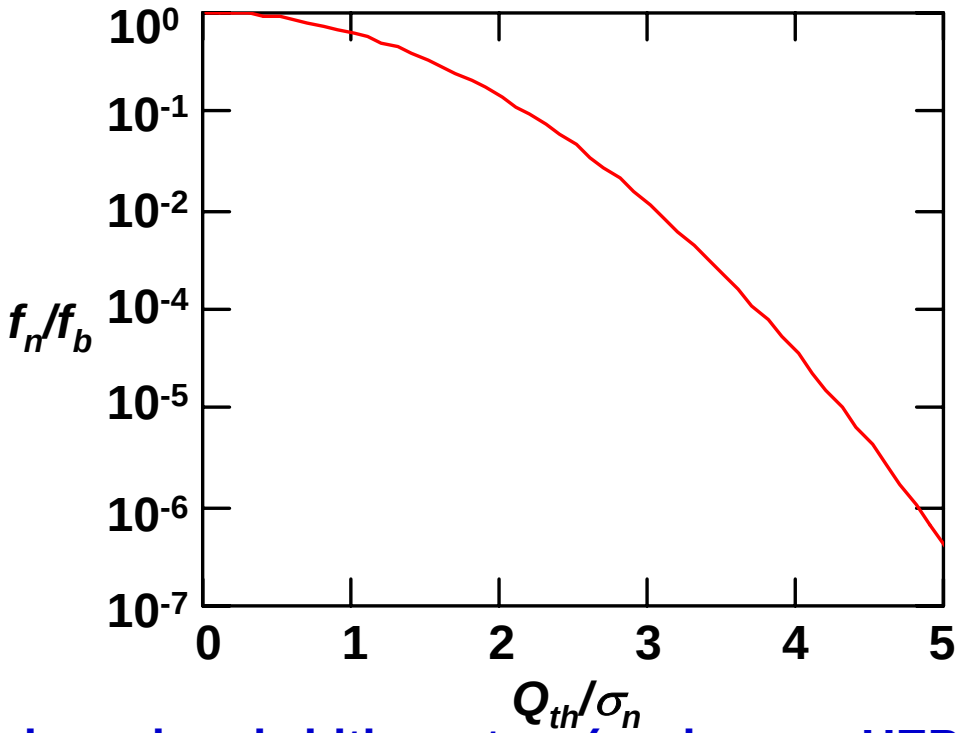
Noise hit rate for a discriminator with bandwidth, f_b

$$f_n = \frac{1}{\sqrt{3}} f_b \exp\left(\frac{-Q_{th}^{\,2}}{2\sigma_n^{\,2}}\right)$$

Q_{th} = threshold
σ_n = noise

(It can be shown that σ_{th} - the threshold variation - adds to σ_n quadratically on the denominator.)

Noise hit rate for a discriminator with bandwidth, f_b



In a large bandwidth system (such as an HEP experiment) noise and threshold must be well separated to produce clean event information.

The same separation provides practically noise-free images in radiation imaging applications

Pixels for High Energy Physics

- In a high multiplicity environment pixel detectors are crucial to pattern recognition. Technical choices are bound by this.

- In low multiplicity environments signal to noise constraints can be relaxed leading to simpler lower power solutions.

Pixels for Imaging Radiation Detectors

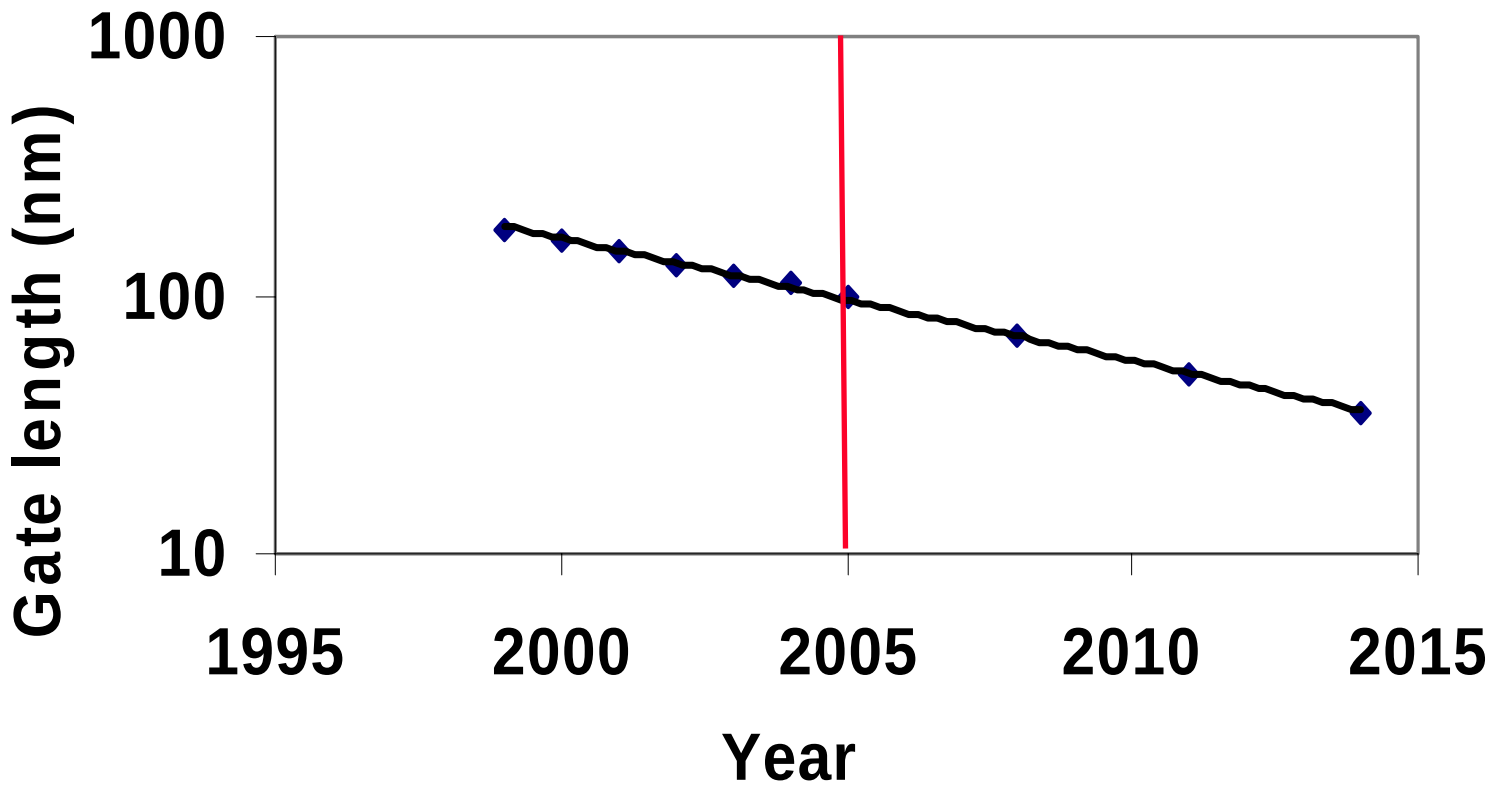
- **Front-end noise is rejected due to high threshold to noise ratio**
- **Detector leakage current can be compensated for pixel-by pixel**
- **Image quality becomes dose rate independent (limited only by background at low rates and by pile up at high rates)**

- **In future CMOS scaling may be useful to make bad detectors more uniform…**

Moore's law and developments in CMOS

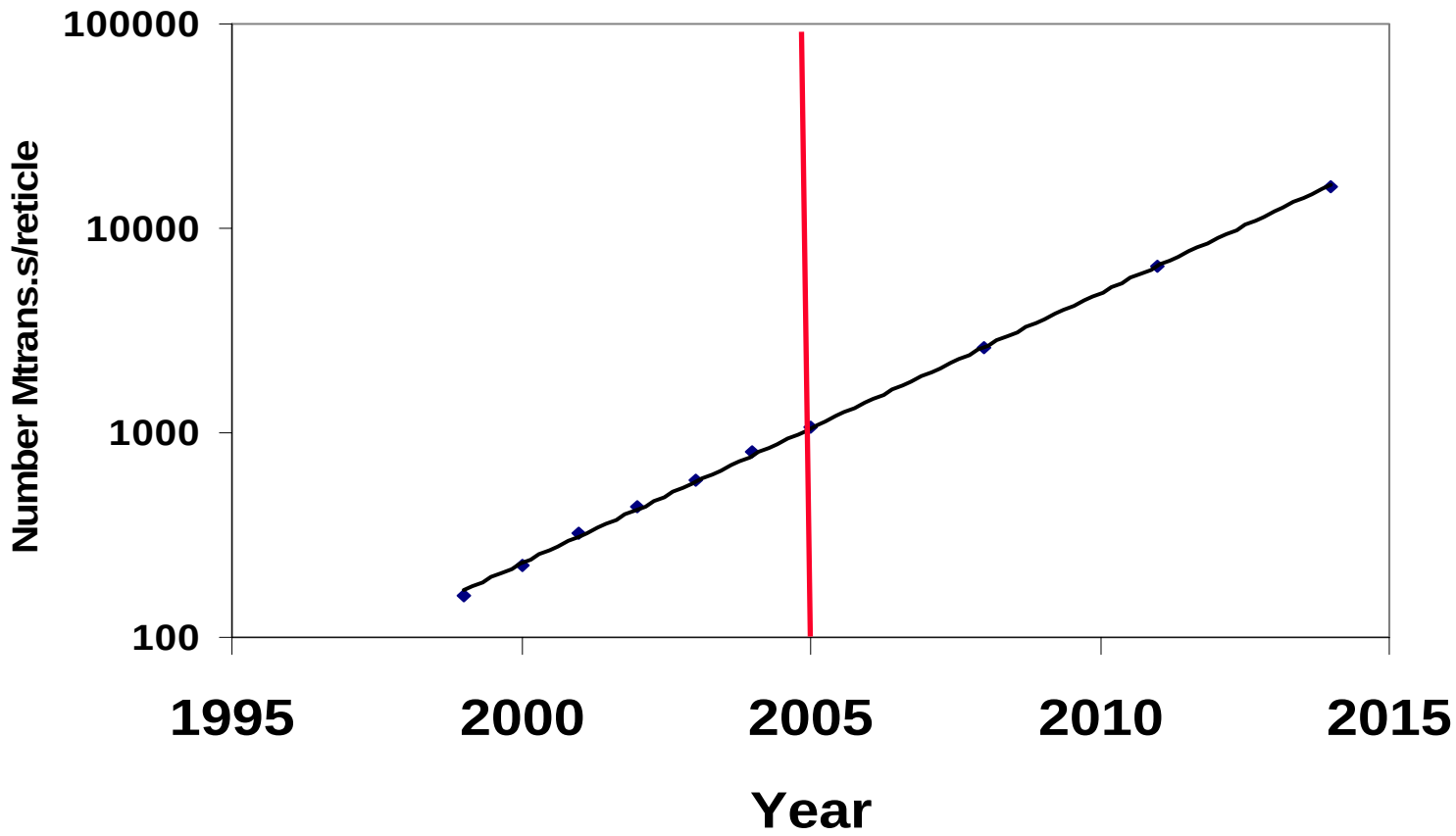
- CMOS is the workhorse for the entire microelectronics industry
- Other technologies (e.g. bipolar, SiGe, GaAs) are used in niche applications but none can compete with CMOS in terms of yield, component density and chip size.
- Experience from the LHC developments indicates that CMOS is the only viable solution for large scale systems

Transistor feature size



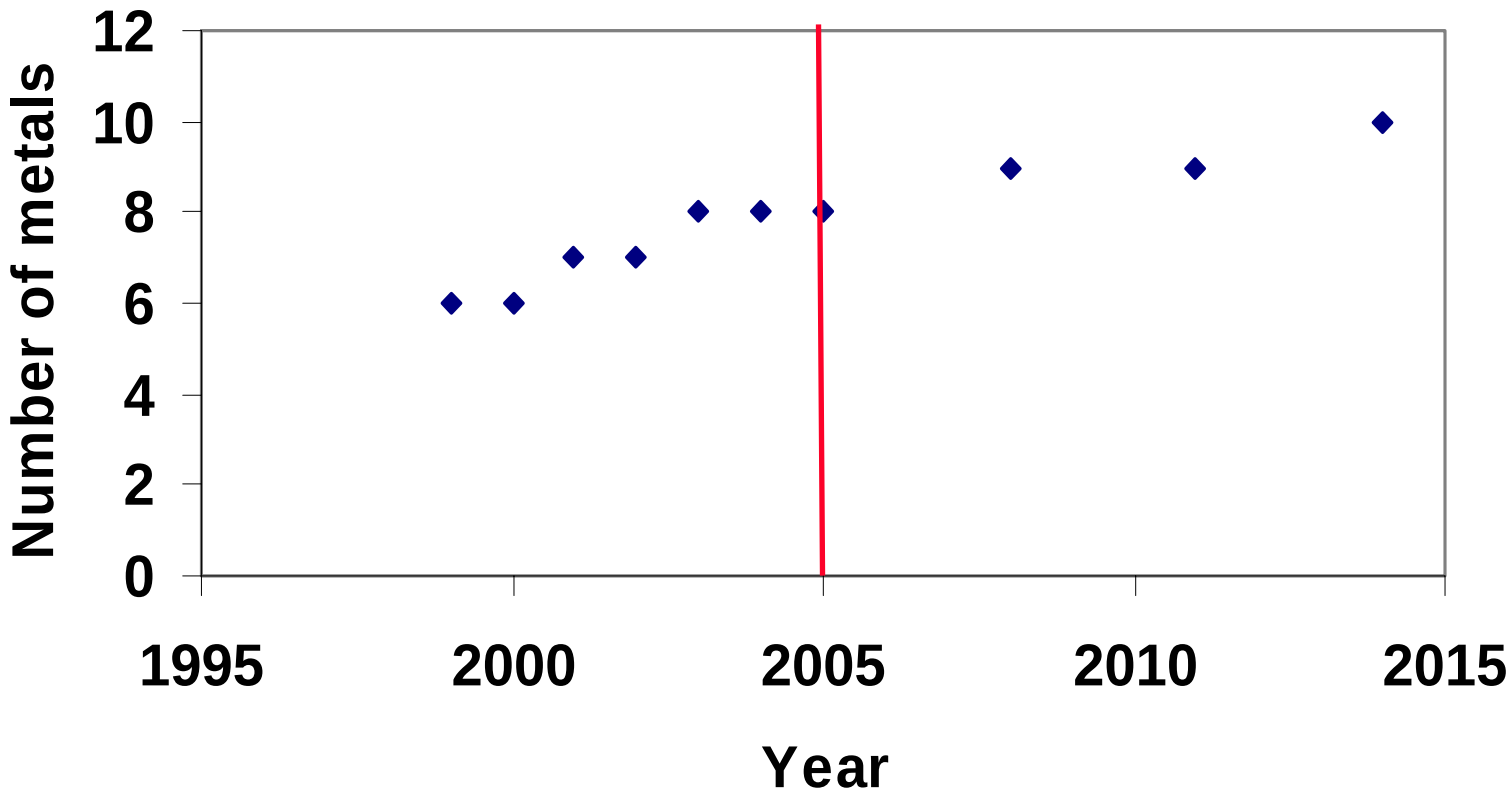
SIA Roadmap 1999

Components per processor chip



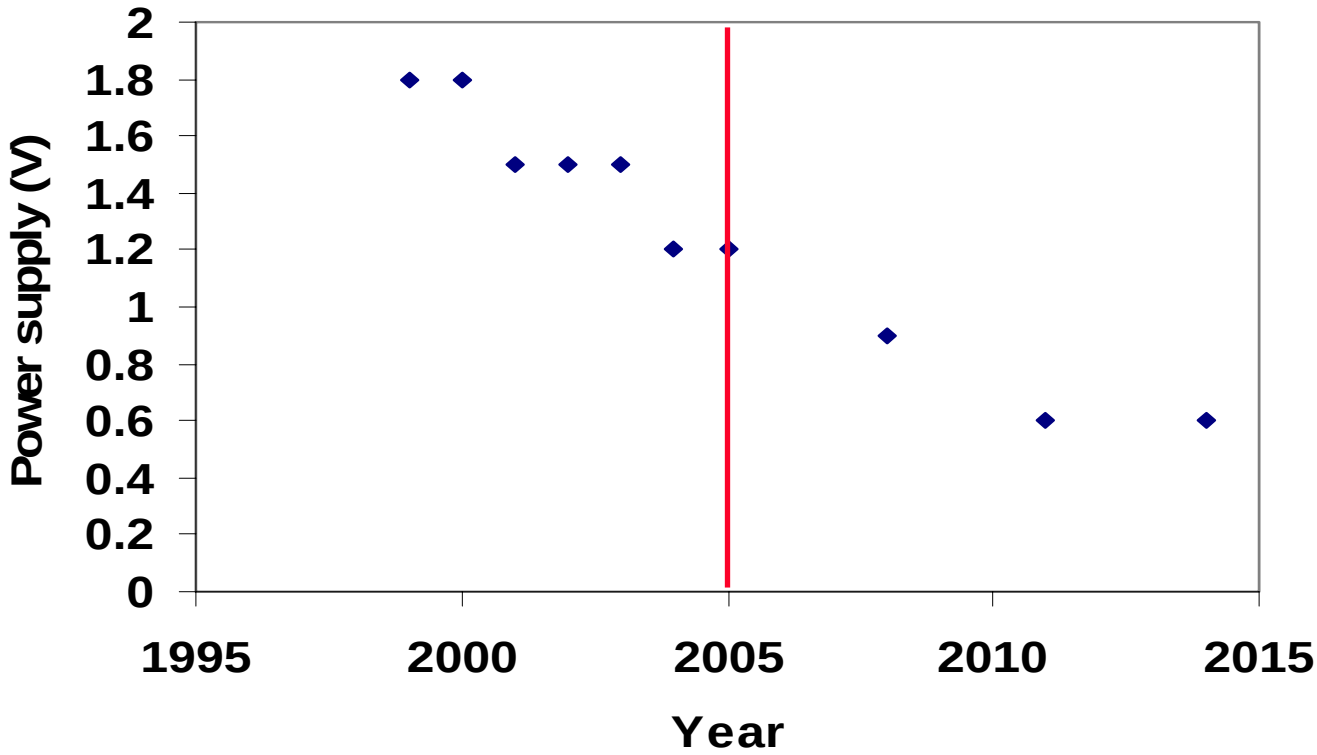
SIA Roadmap 1999

Metal layers



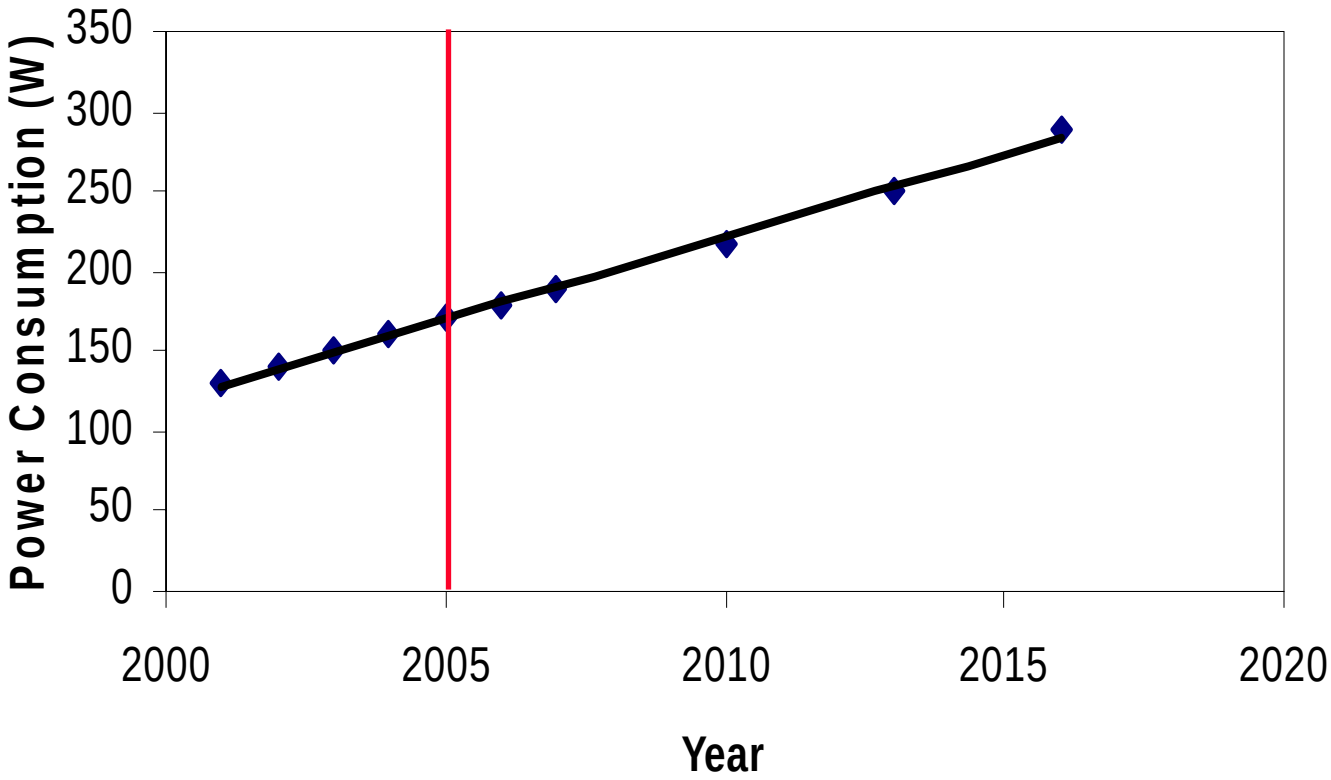
SIA Roadmap 1999

Power supplies



SIA Roadmap 1999

Power per processor chip



SIA Roadmap 2001

Design Considerations for pixel chip design

Noise should be minimized

series noise

$$ENC_d^2 \propto \frac{C_t^2}{g_m \tau_s}$$

high g_m (! power)

parallel noise

$$ENC_o^2 \propto I_o \tau_s$$

fast shaping

Preamp and discriminator should be fast

$$t_r \propto \frac{C_t}{g_m} \frac{(C_L + C_f)}{C_f}$$

high g_m (! power!)

Transistor matching

$$\sigma^2(V_{th}) \propto \frac{A^2}{WL}$$

! good matching requires large area transistors

Design Implications of further scaling- general - positive aspects

I/f noise decreases

Matching improved for constant dimensions:

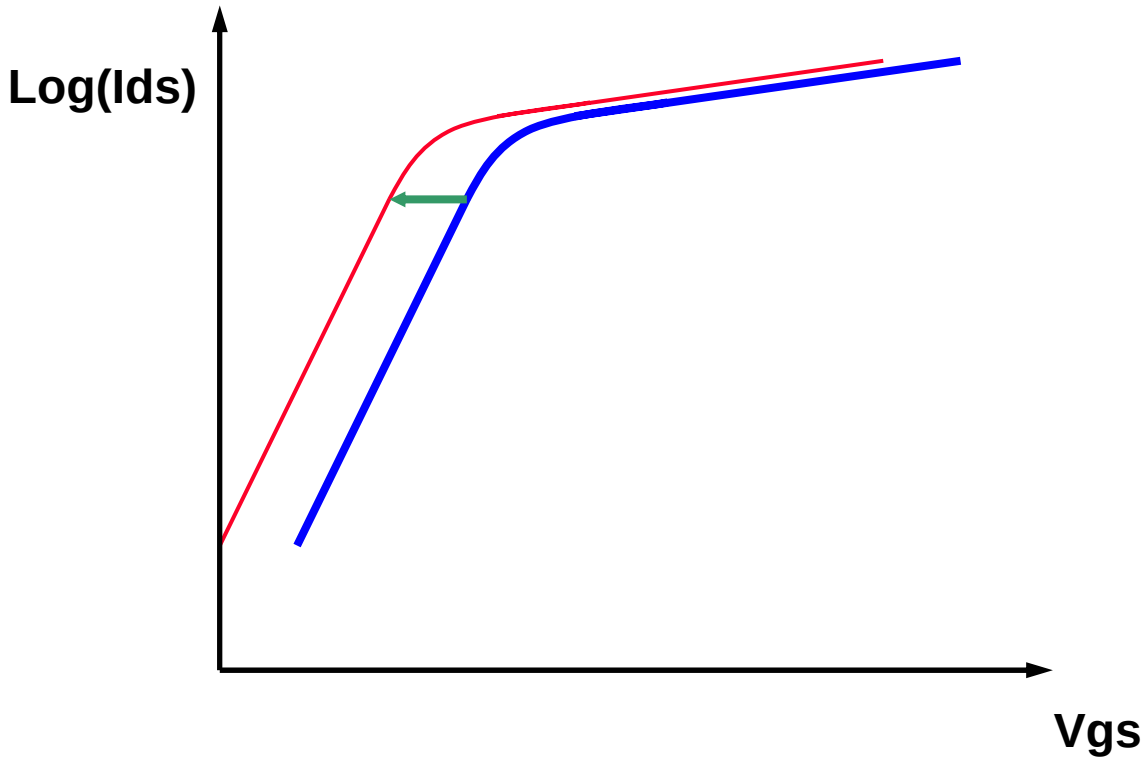
$$\sigma^2(V_{th}) \propto \frac{A_v^2}{WL}$$

A_v = 1mV per nm of gate thickness micron*

Many more digital transistors per unit area

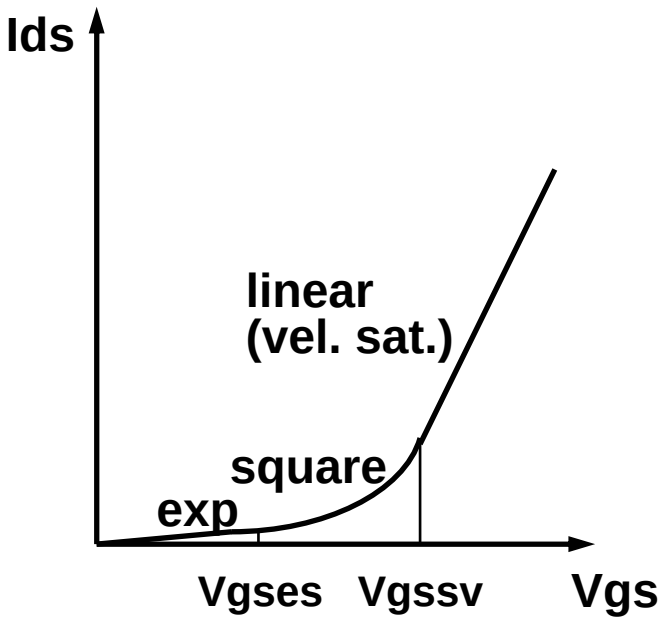
*** H.Tuinhout, "Matching of NMOS Transistors," Short Course on Deep Submicron Modeling and Simulation, 12-15 Oct. 1998, EPFL, Lausanne, Switzerland**

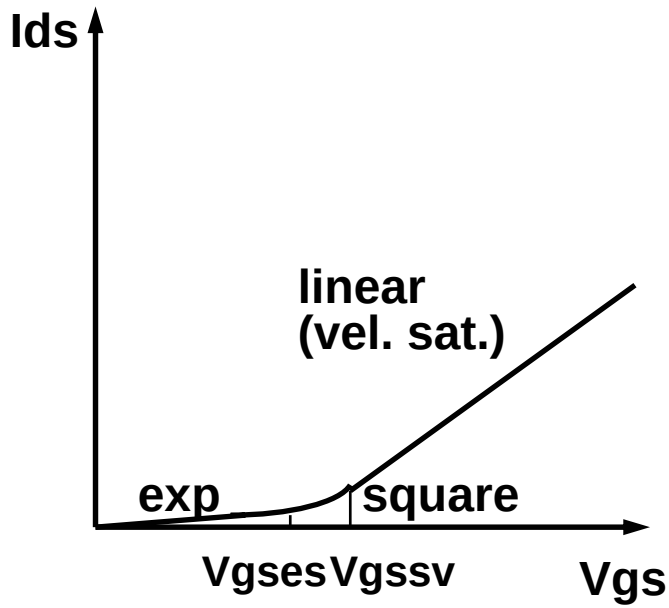
Design Implications of further scaling- general - Vt reduction



Vt goes down, but weak inversion slope is constant.
Dynamic range limited

Design Implications of further scaling- general - square law region disappears





$V_{gses} - V_t = 2nkT/q$

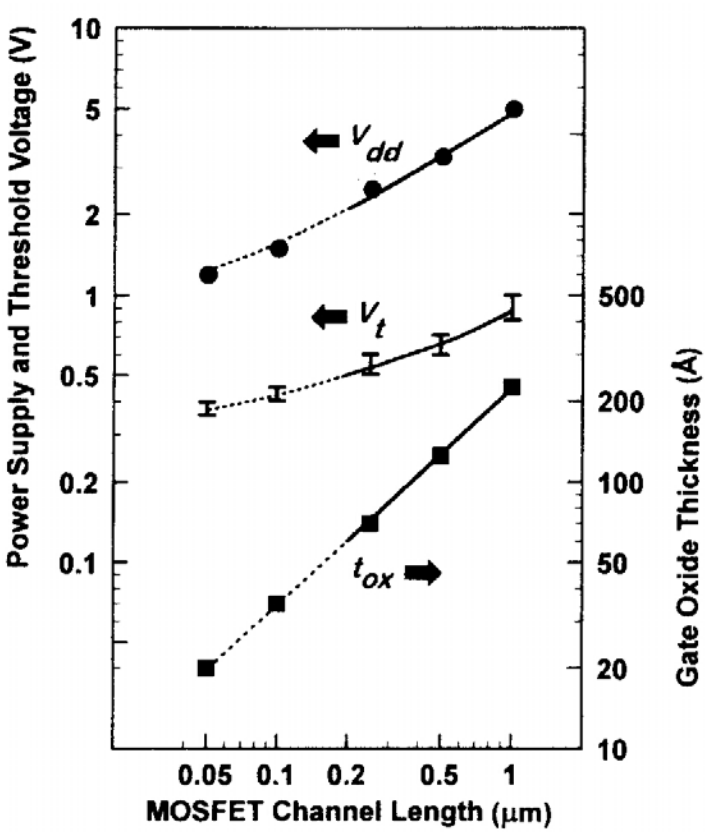
$V_{gssv} - V_t = 4nLv_{sat}/u$

Input devices will operate in Weak Inversion

$g_m = I_d/nU_T$

W.Sansen, "Low Voltage, low power analog CMOS design," Short Course on low voltage, low power analog CMOS IC design, June 21-25 1999, EPFL, Lausanne, Switzerland.

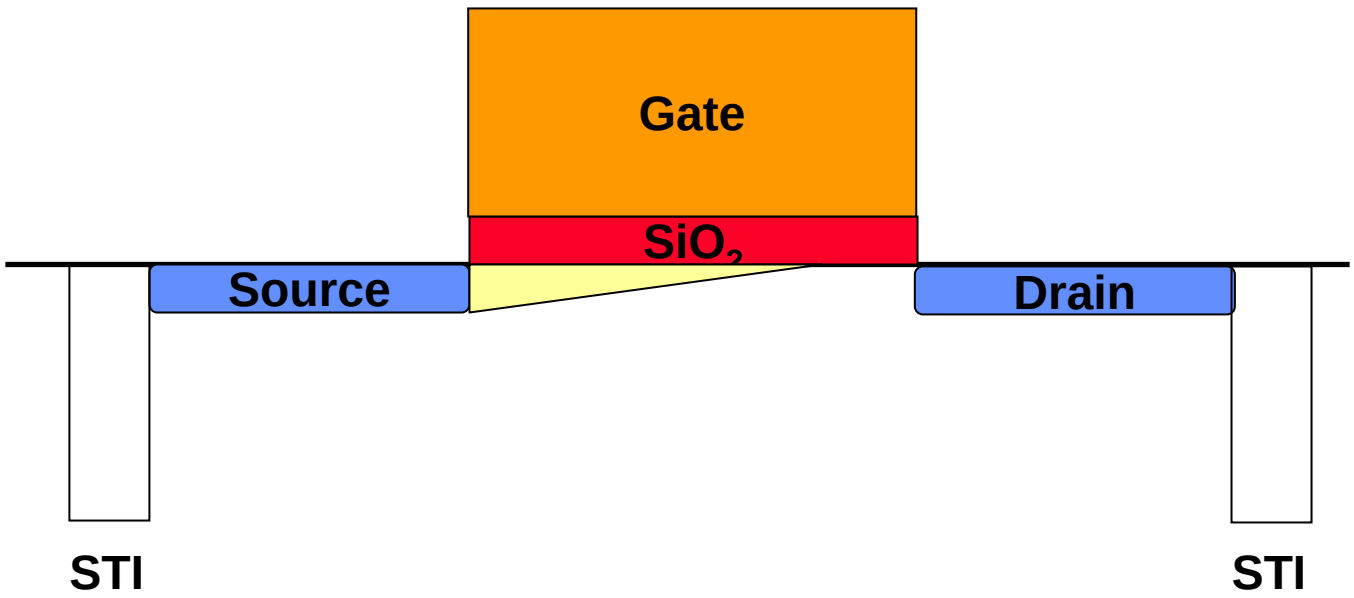
Power Supply Voltage and Transistor Threshold



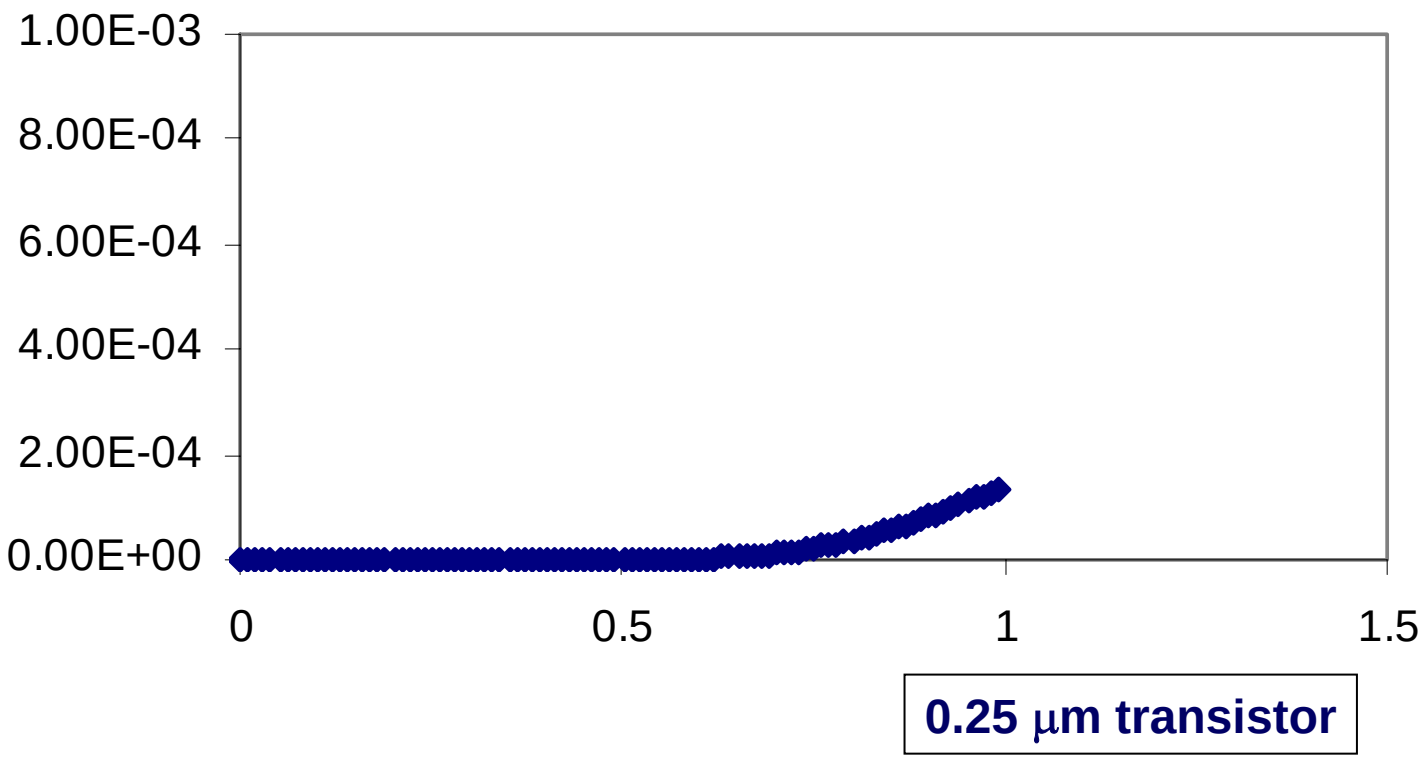
Stacking of transistors in one branch becomes difficult

Y.Taur, D.A.Buchanan, W.Chen et al., "CMOS Scaling into the Nanometer Regime, Proceedings IEEE, Vol 85 no4, 1997, pp.486-504

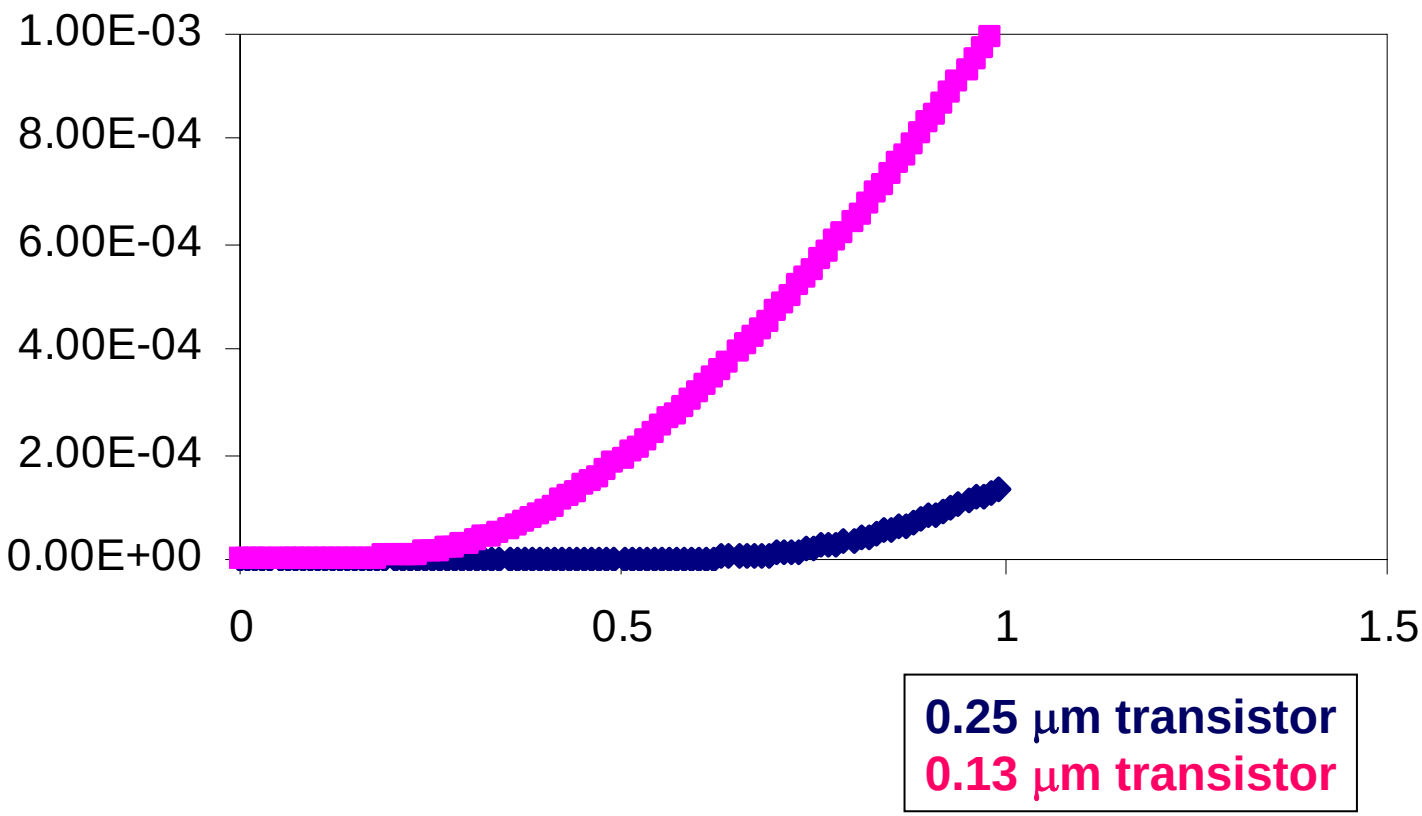
Profile of a CMOS Tansistor



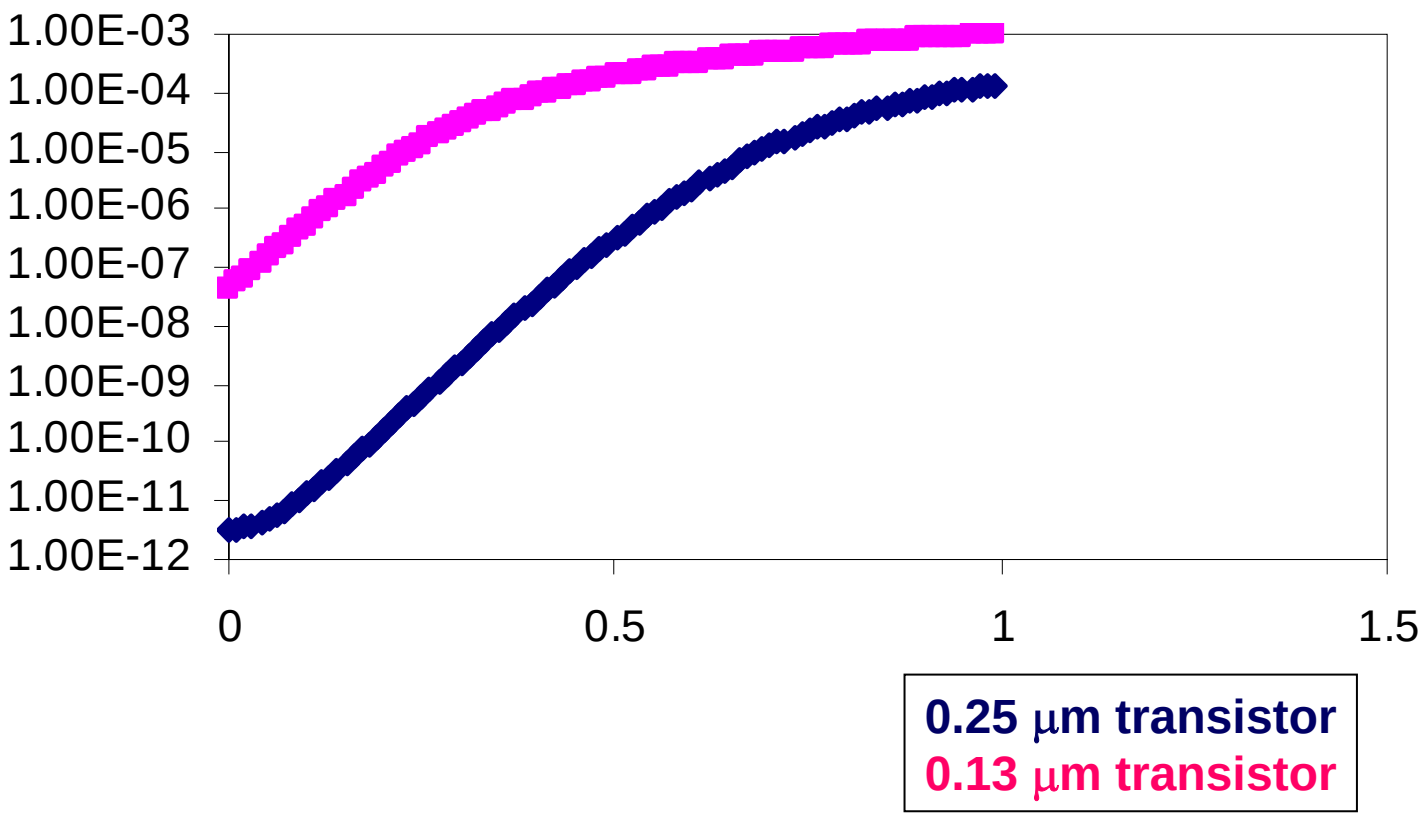
I_{DS} vs V_{GS}


1.00E-03
8.00E-04
6.00E-04
4.00E-04
2.00E-04
0.00E+00
0
0.5
1
1.5
0.25 μm transistor

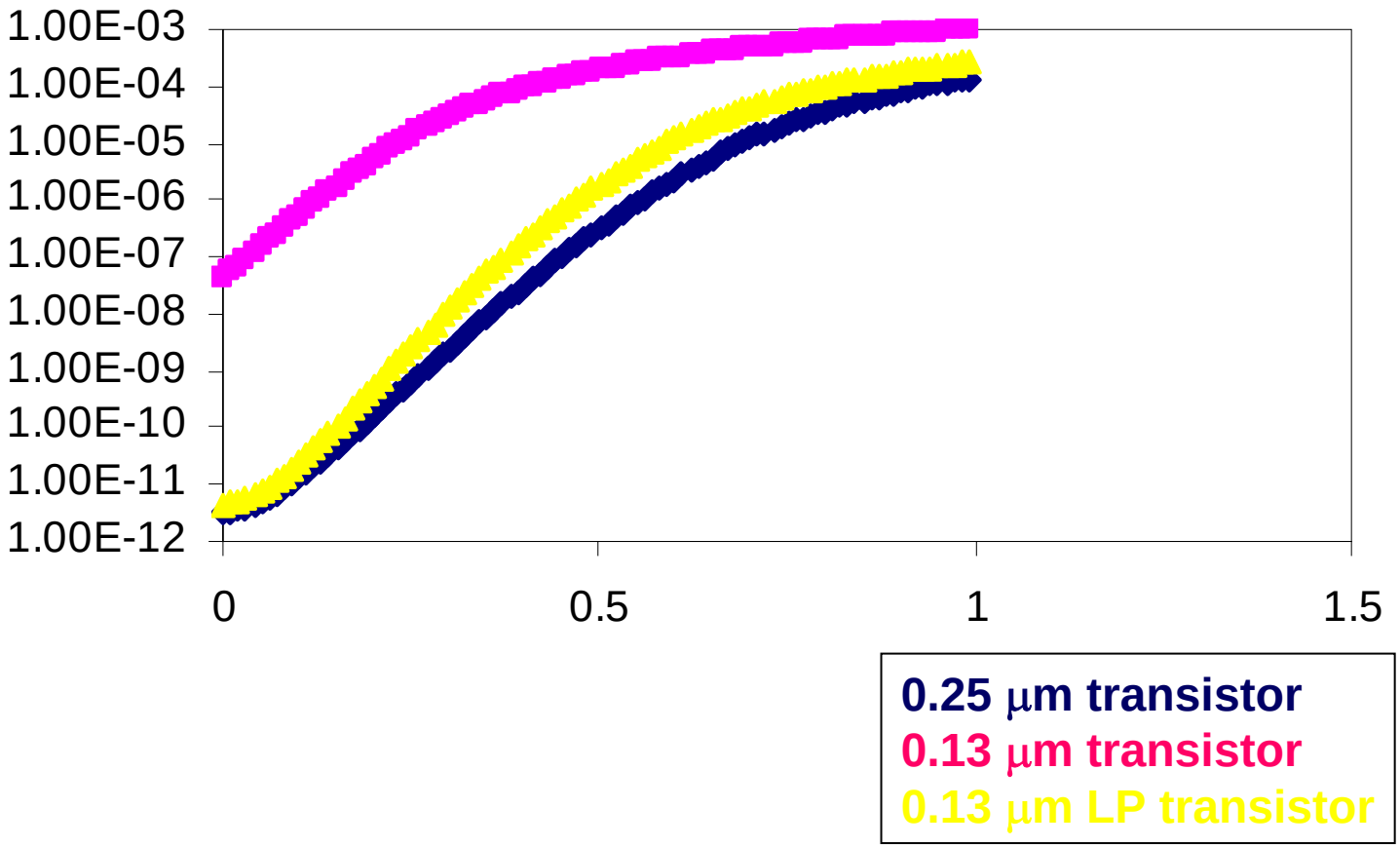
I_{DS} vs V_{GS}


1.00E-03
8.00E-04
6.00E-04
4.00E-04
2.00E-04
0.00E+00
0
0.5
1
1.5
0.25 μm transistor
0.13 μm transistor

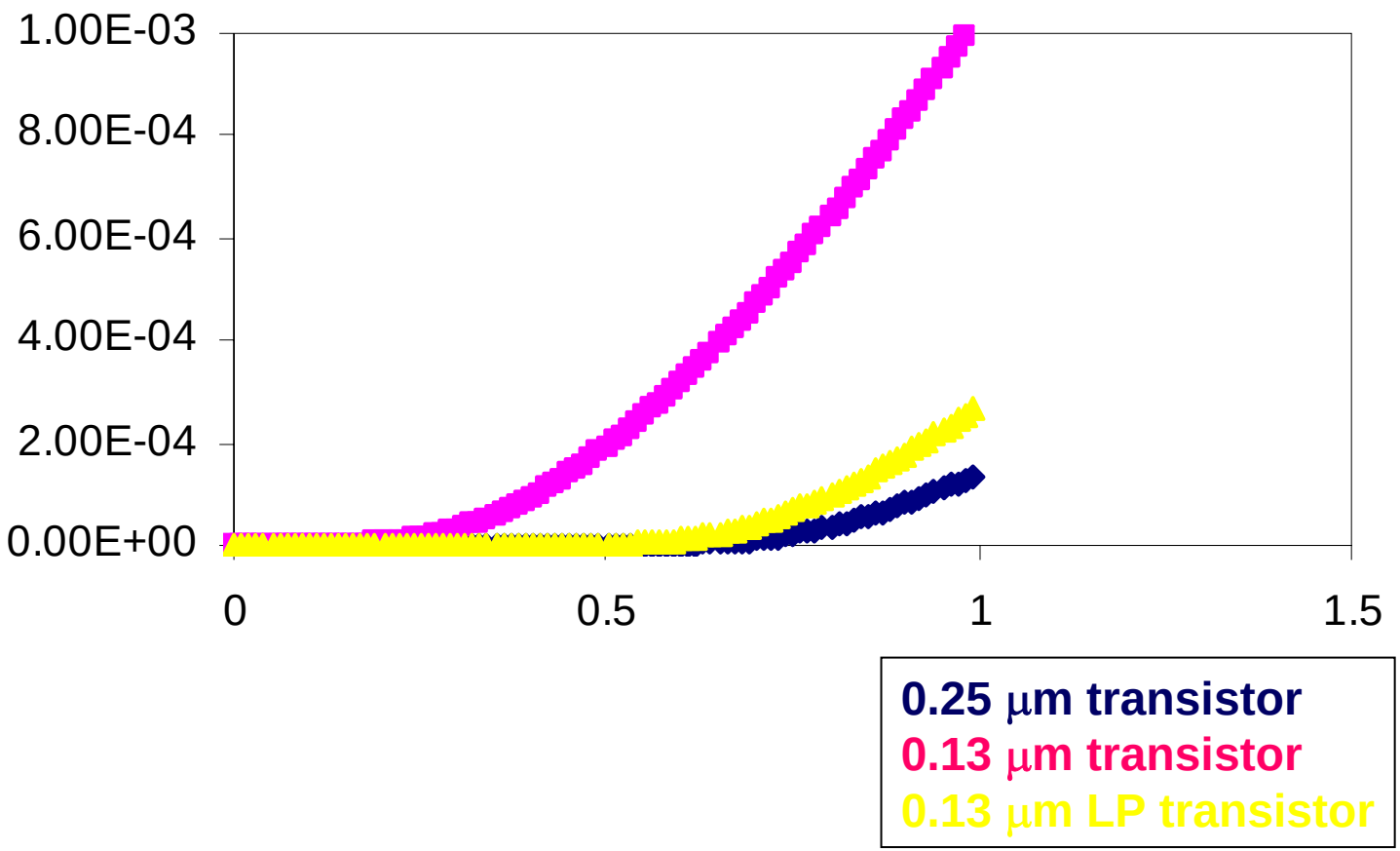
Log (I_{DS}) vs V_{GS}



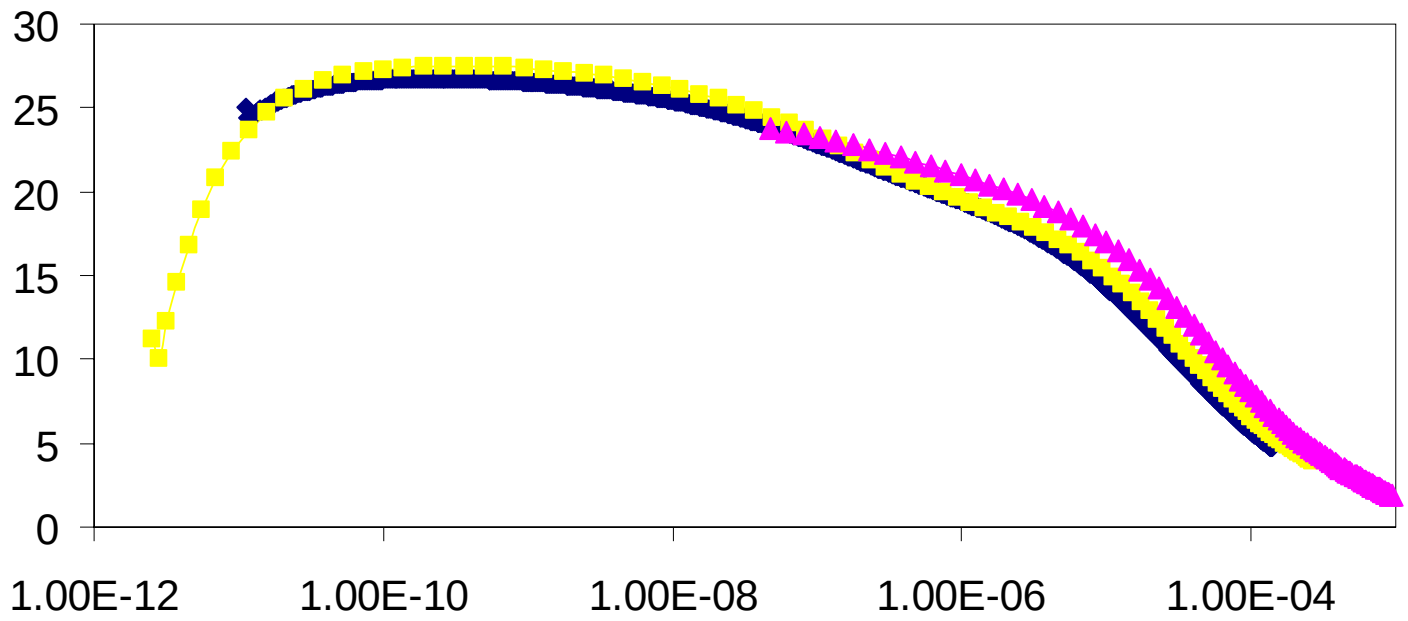
Log (I_{DS}) vs V_{GS}



I_{DS} vs V_{GS}

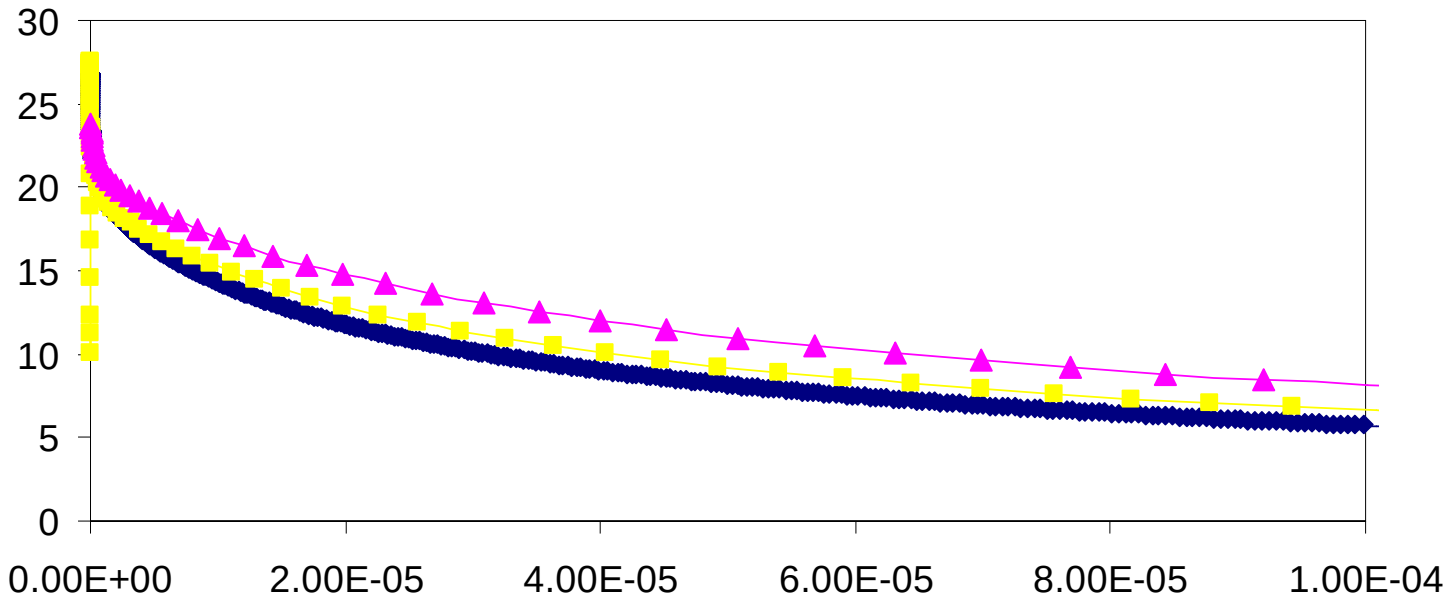

1.00E-03
8.00E-04
6.00E-04
4.00E-04
2.00E-04
0.00E+00
0
0.5
1
1.5
0.25 μm transistor
0.13 μm transistor
0.13 μm LP transistor

g_m/I_{DS} vs log (I_{DS})



0.25 μm transistor
0.13 μm transistor
0.13 μm LP transistor

g_m/I_{DS} vs log (I_{DS})



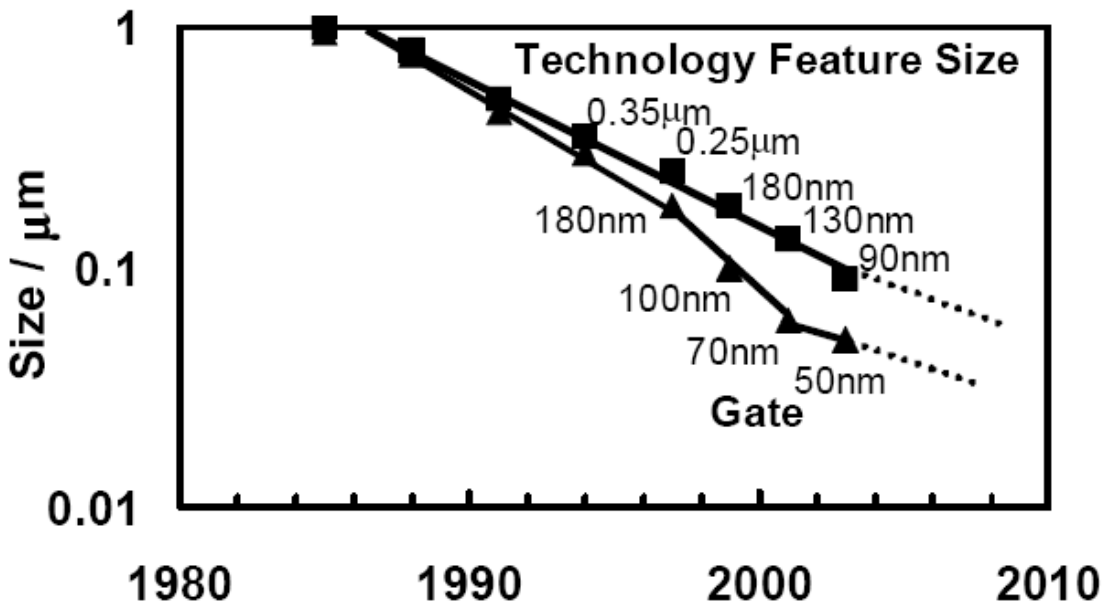
0.25 μm transistor
0.13 μm transistor
0.13 μm LP transistor

CMOS design at present

- Moving from 0.25 μm to 0.13 μm enables many more transistors to be implemented on a single pixel
- Multiple thresholds and counters are feasible even on a relatively small pixel
- Analogue front-end design is complicated by inherent limitations of the fastest devices and power supply limitations

Present day leading edge processes -1

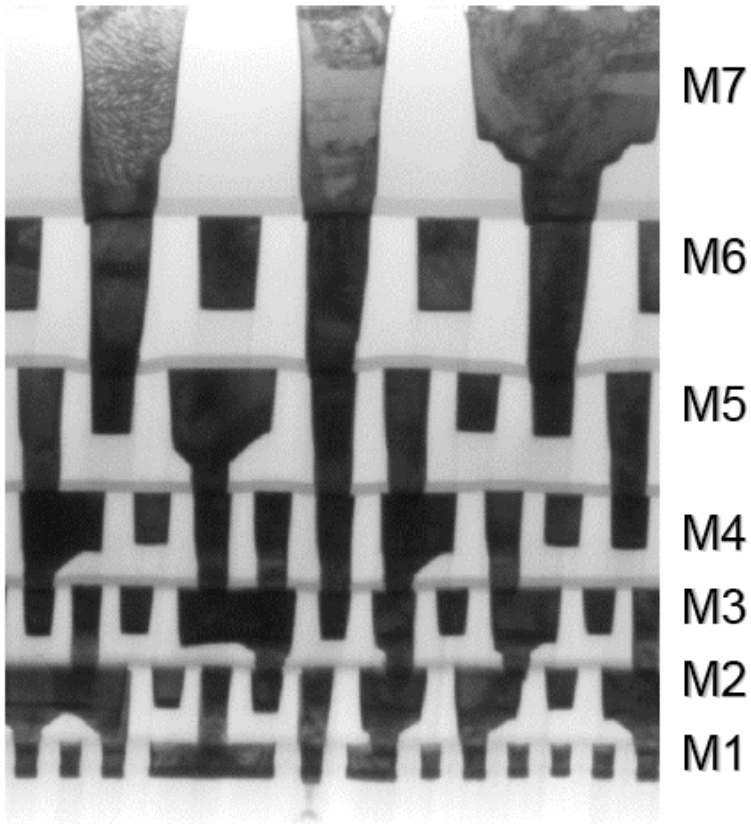
Intel



[S. Thomson et al., IEDM, San Francisco, 8-11 Dec. 2002 (next 2 slides)]

Present day leading edge processes -2

Intel



Present day CMOS - 3

A 90nm CMOS Device Technology ….
TSMC

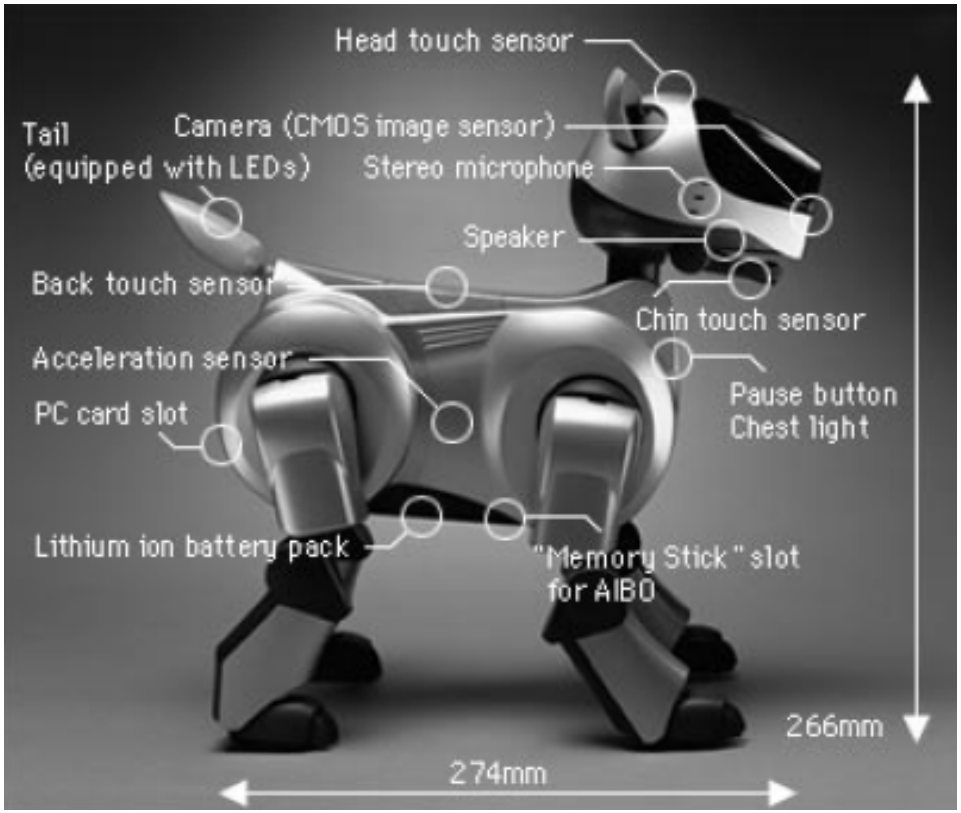
TSMC Process	LP			G			HS		I/Os		
	Low-Vt	Std-Vt	High Vt	Low-Vt	Std-Vt	High Vt	Std-Vt	High-Vt			
V_{dd} (V)	1.2			1 (1.2)			1		1.8	2.5	3.3
T_{ox} (nm) [EOT]	22			16			<14		28	~53	~70
L_g (um)	80			65			45/50	50/55	145	265	365
I_{ds} (uA/um)	540/250	420/180	370/130	755/335 (995/460)	640/280 (865/400)	520/215 (750/320)	830/380	670/310	660/300	580/290	580/290
I_{off} (nA/um)	0.4	0.015	0.004	50 (75)	5 (7.5)	1 (1.5)	75	10	<300	<300	<300
J_g (A/um^2)	100p/30p			2.4n/1n (6n/2.4n)			0.3-1u		<5p	<1f	<<1f
C_i (fF/um^2)	1.3/1.2			0.85/0.95							
Inverter delay (ps)	15	21	26	9.5 (8.4)	11.3 (9.5)	14.5(11.6)	7.9	10.5	<23	<32	<42

I_{ds} (off) = 50 nA/μm of gate length
I_g (leak) = 2.4nA/μm² of gate area (5A/cm² !)

[C.C. Wu et al., IEDM, San Francisco, 8-11 Dec. 2002]

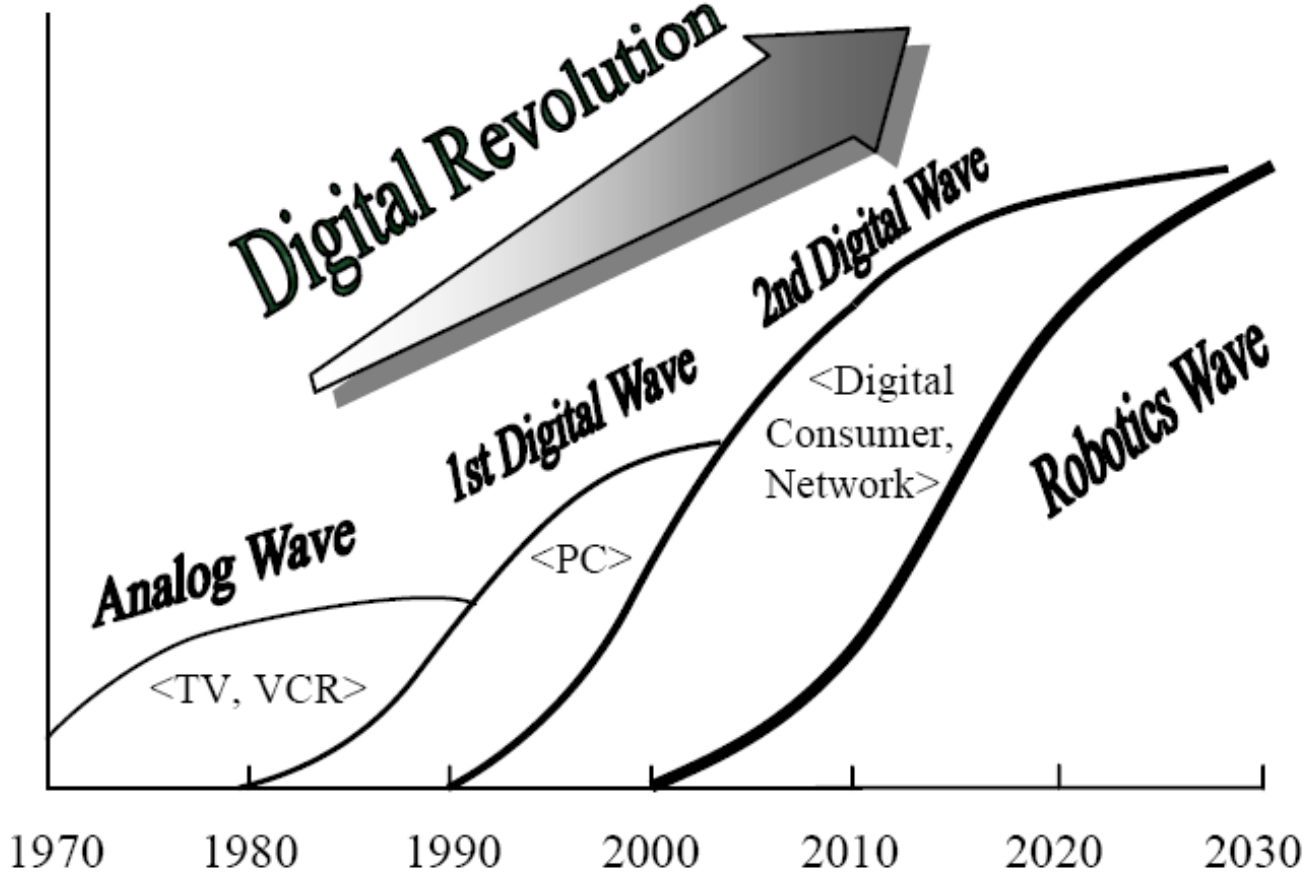
Technology drivers….

Household friends…

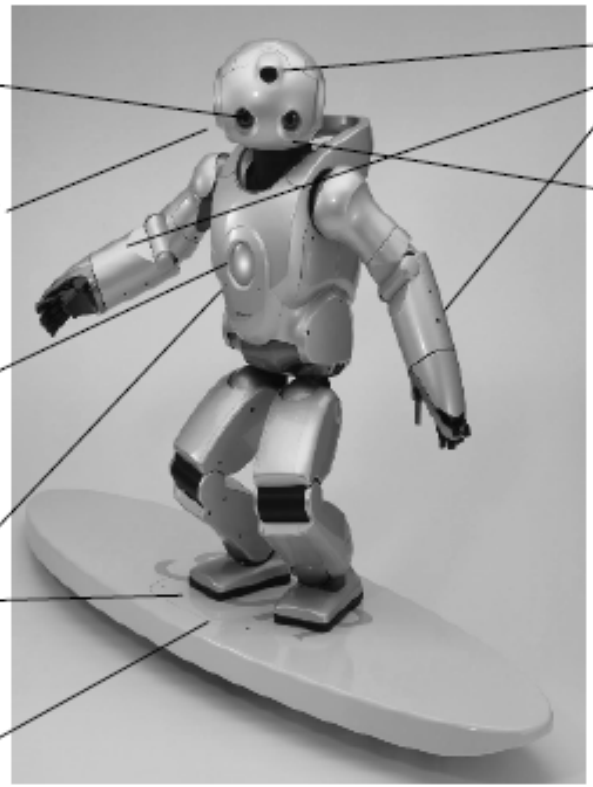


T. Kamimoto and T.T.Doi, IEDM, San Francisco, 8-11 Dec. 2002 (next 4 slides)]

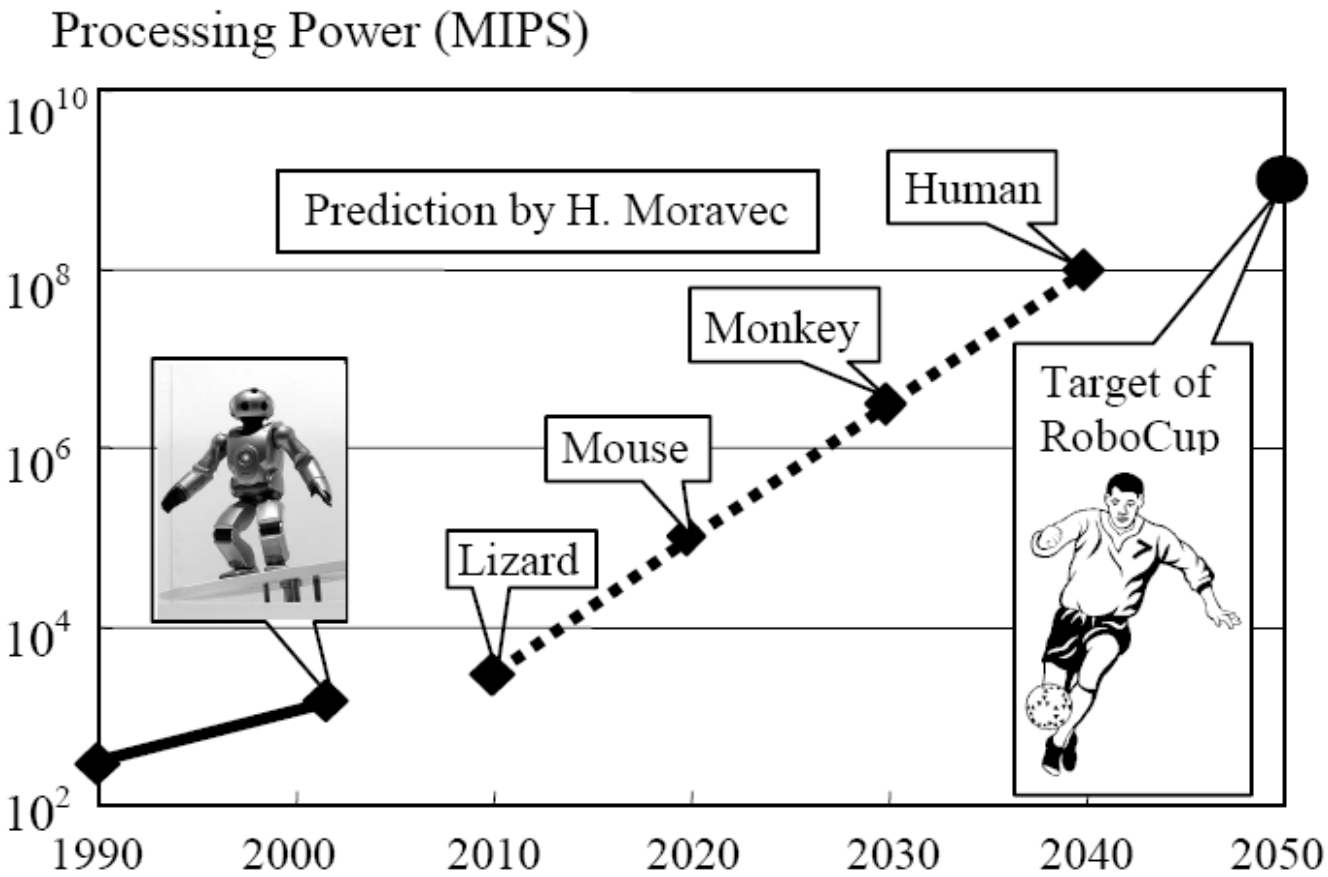
The Sony Vision - 1



And they don't stop at animals…



The Sony Vision - 2



A team of Sony robots should beat the football World Cup champions in 2050….

CMOS scaling - challenges

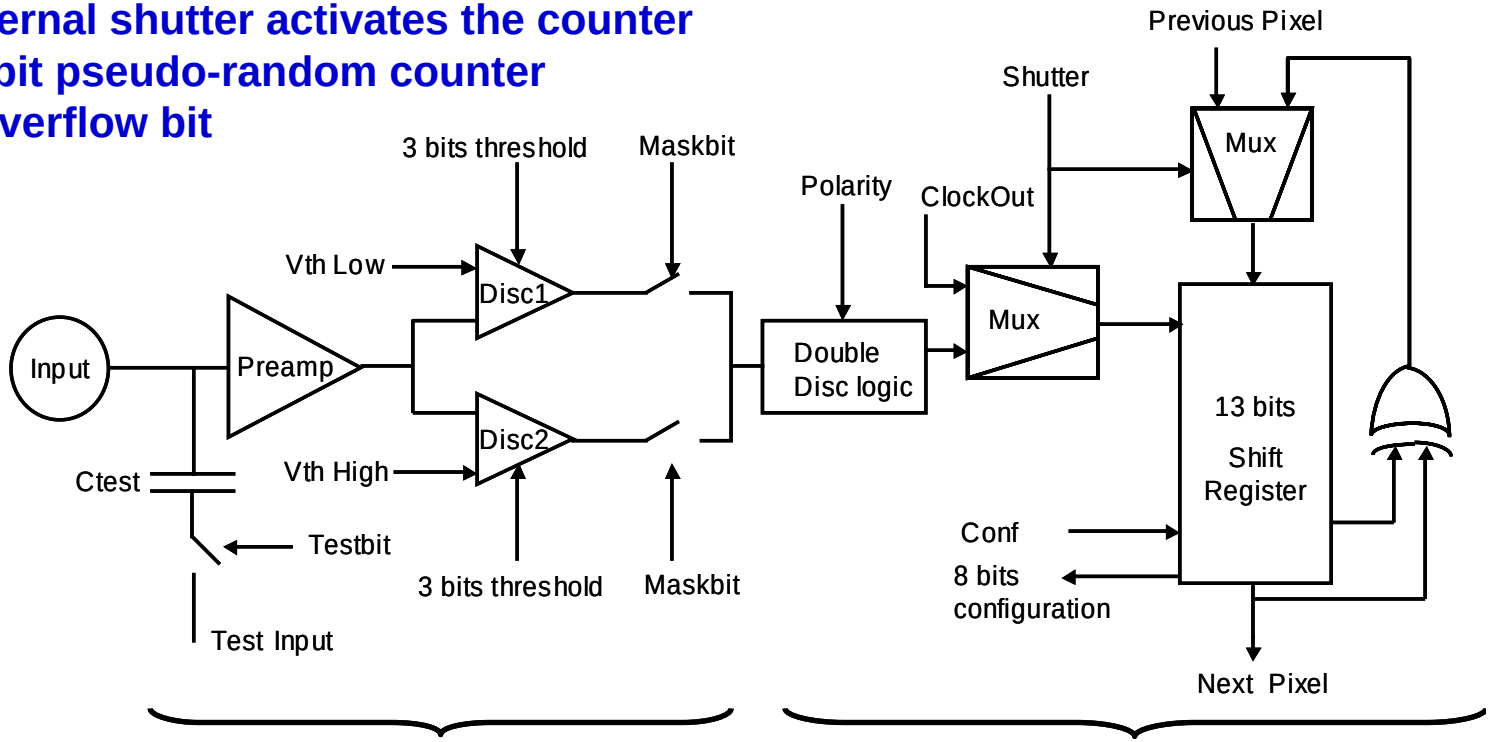
Front ends:
New front-end circuit topologies are being developed
Designers must find a way through a zoo of possible devices and technology options

Digital circuits:
These become more complicated with every generation.
Existing tools don't cover well high density mixed-mode design

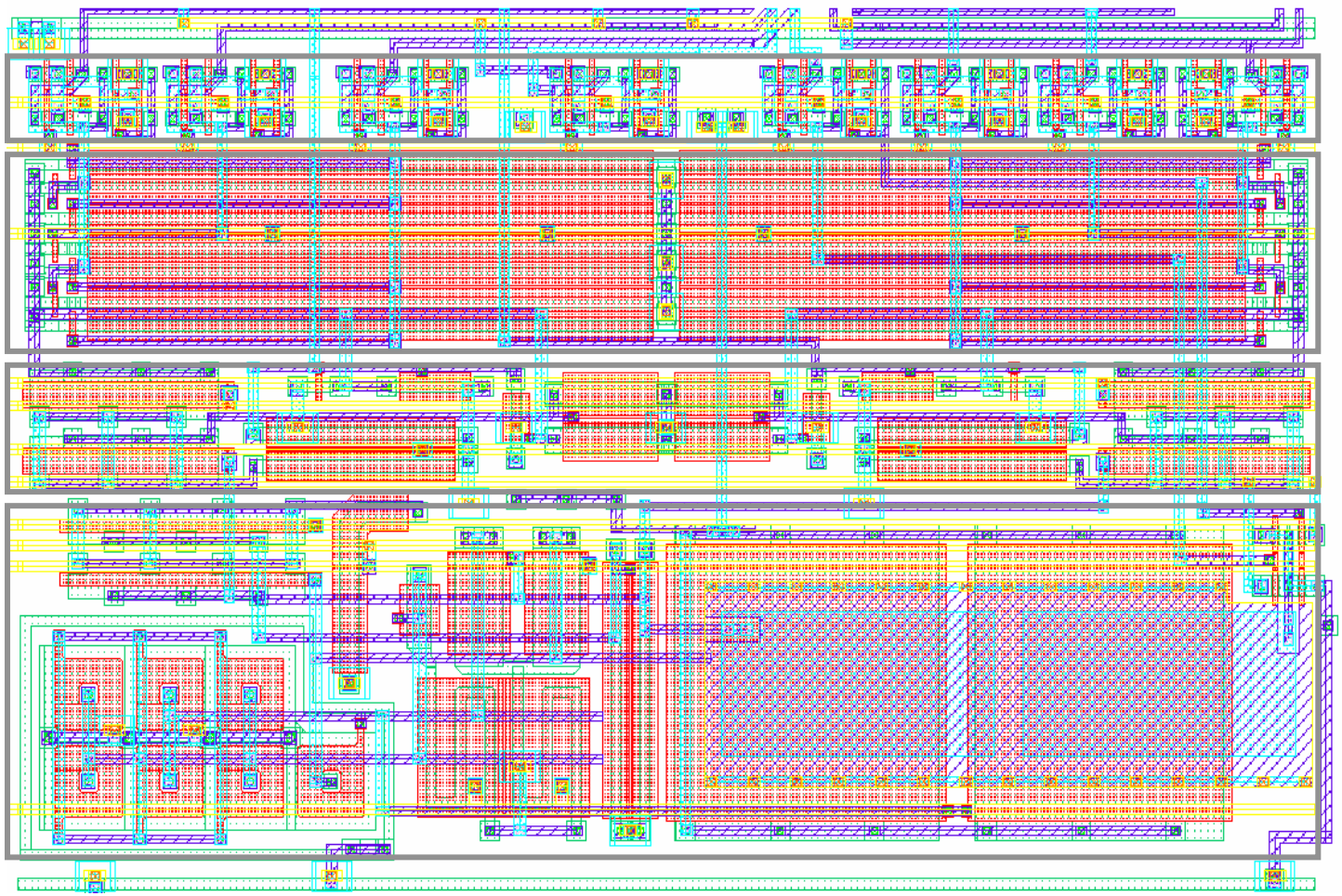
Technology:
Prototyping costs are enormous

Medipix2 Cell Schematic

Charge sensitive preamplifier with individual leakage current compensation
2 discriminators with globally adjustable thresholds
3-bit local fine tuning of the threshold per discriminator
1 test and1 mask bit
External shutter activates the counter
13-bit pseudo-random counter
1 Overflow bit



Medipix2 Pixel (Analog)



8 Config Latches

Threshold Adjust

- 7 equal transistors:
  - Bit2: 4 Trts
  - Bit1: 2 Trts
  - Bit0: 1 Trt

Disc

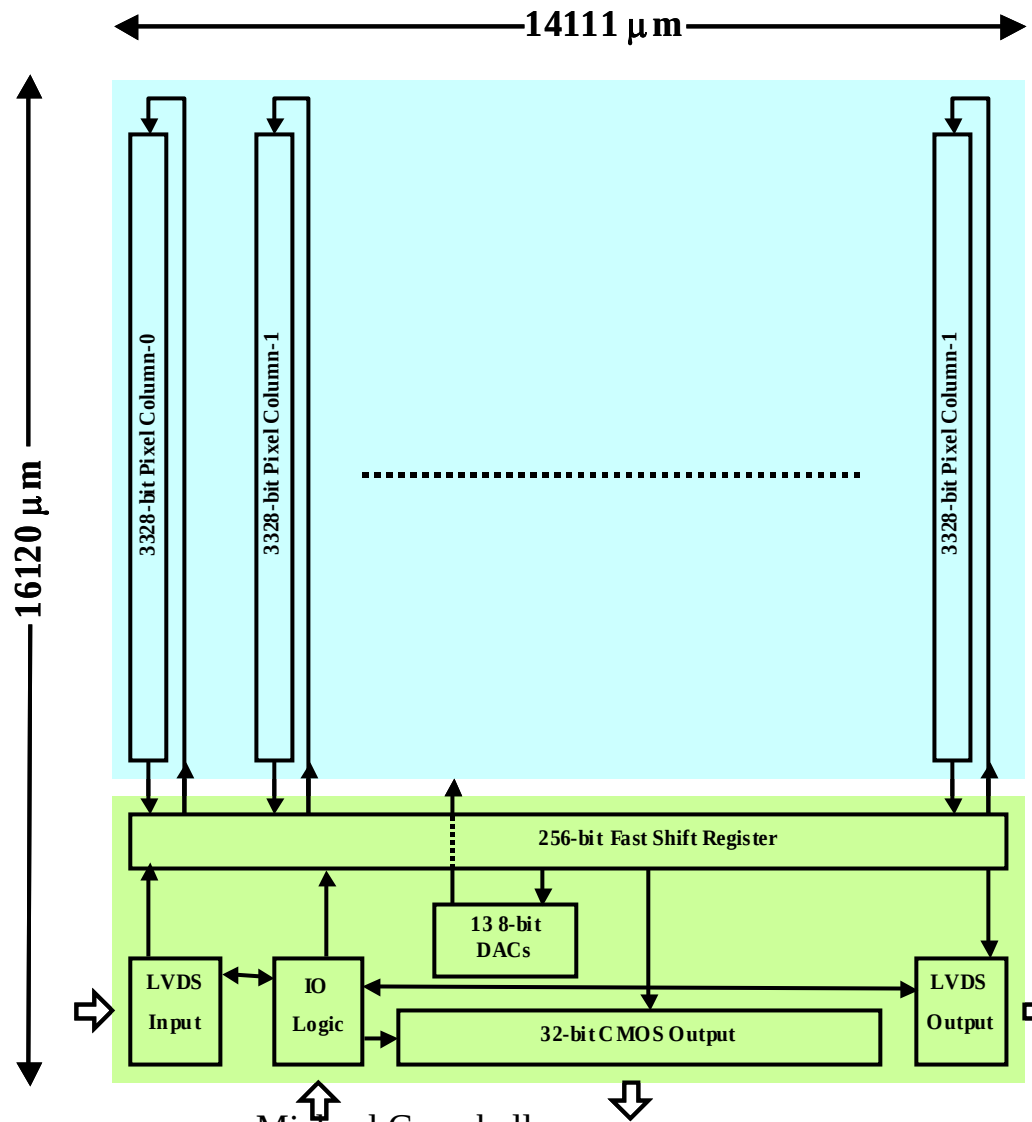
- Idisc ≅ 3xIDISC
- Analog output

Amplifier

- Ikrum Mirroring
- CL ≅ 1.3pF
- Cfb ≅ 8fF
- CTest ≅ 8fF
- Iamp ≅ 1uA
- Ikrum ≅ 15nA

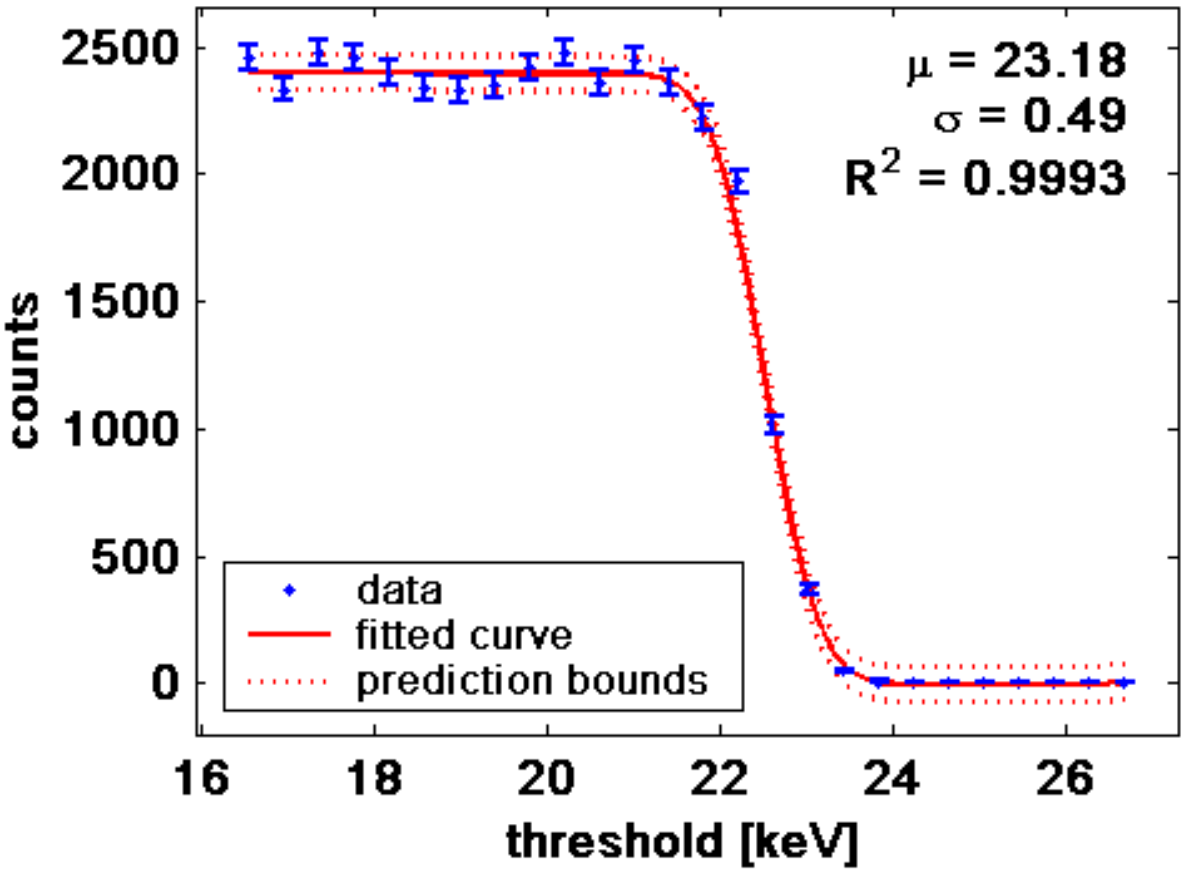
Medipix2 Chip Architecture

256 x 256 pixels

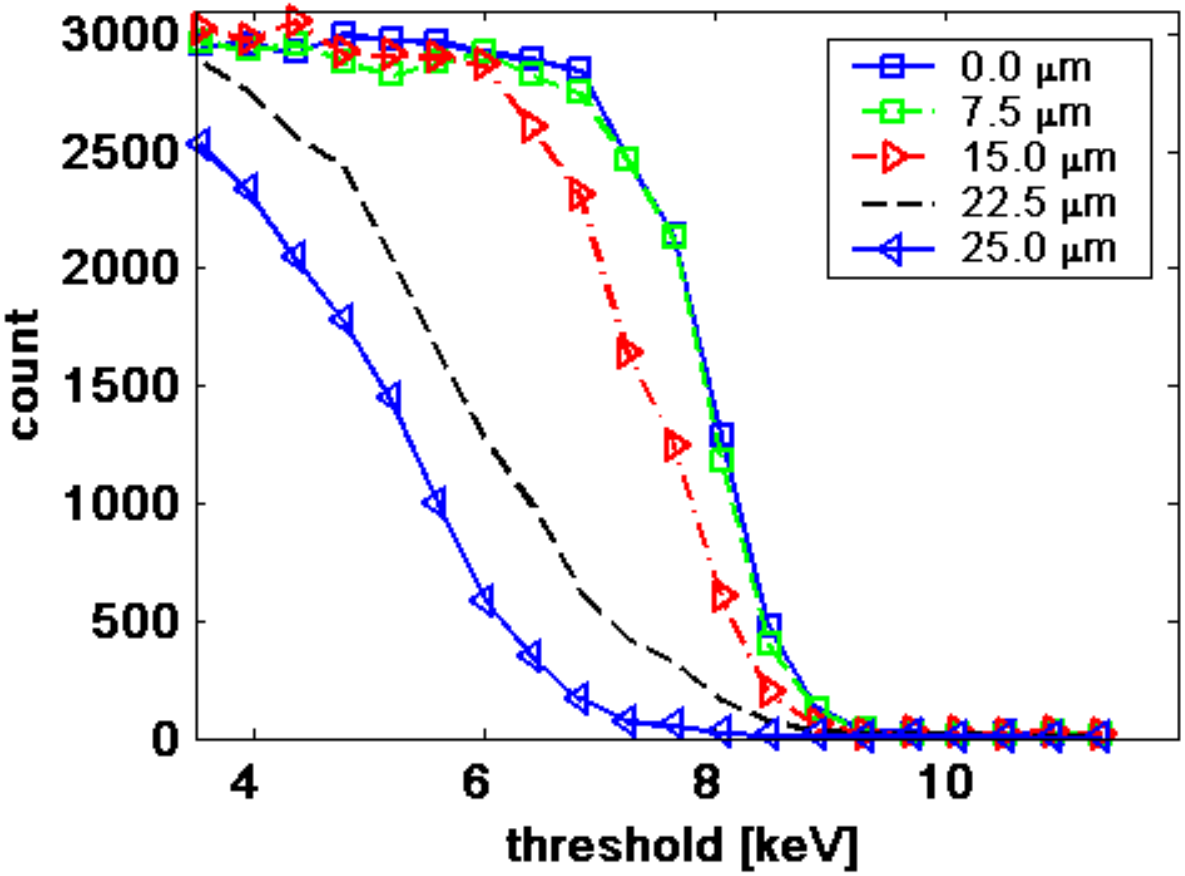


10 ms readout time

Threshold scan with a pencil beam in pixel centre

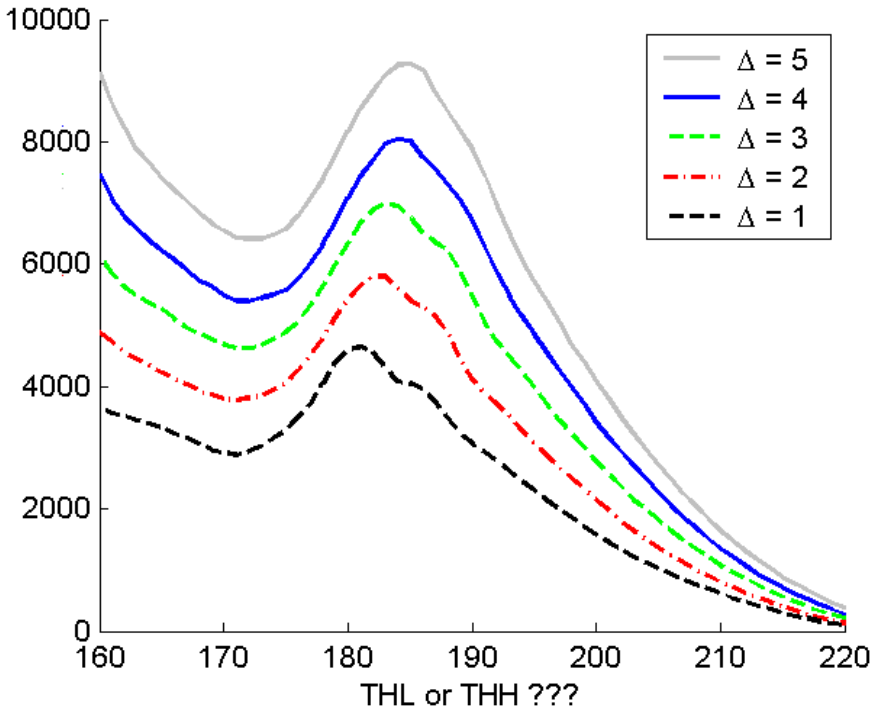


Threshold scan with a pencil beam at various distances from pixel centre



Spectrum of X-ray source using energy window

Raw sum of counts in all 64 000 pixels versus global threshold

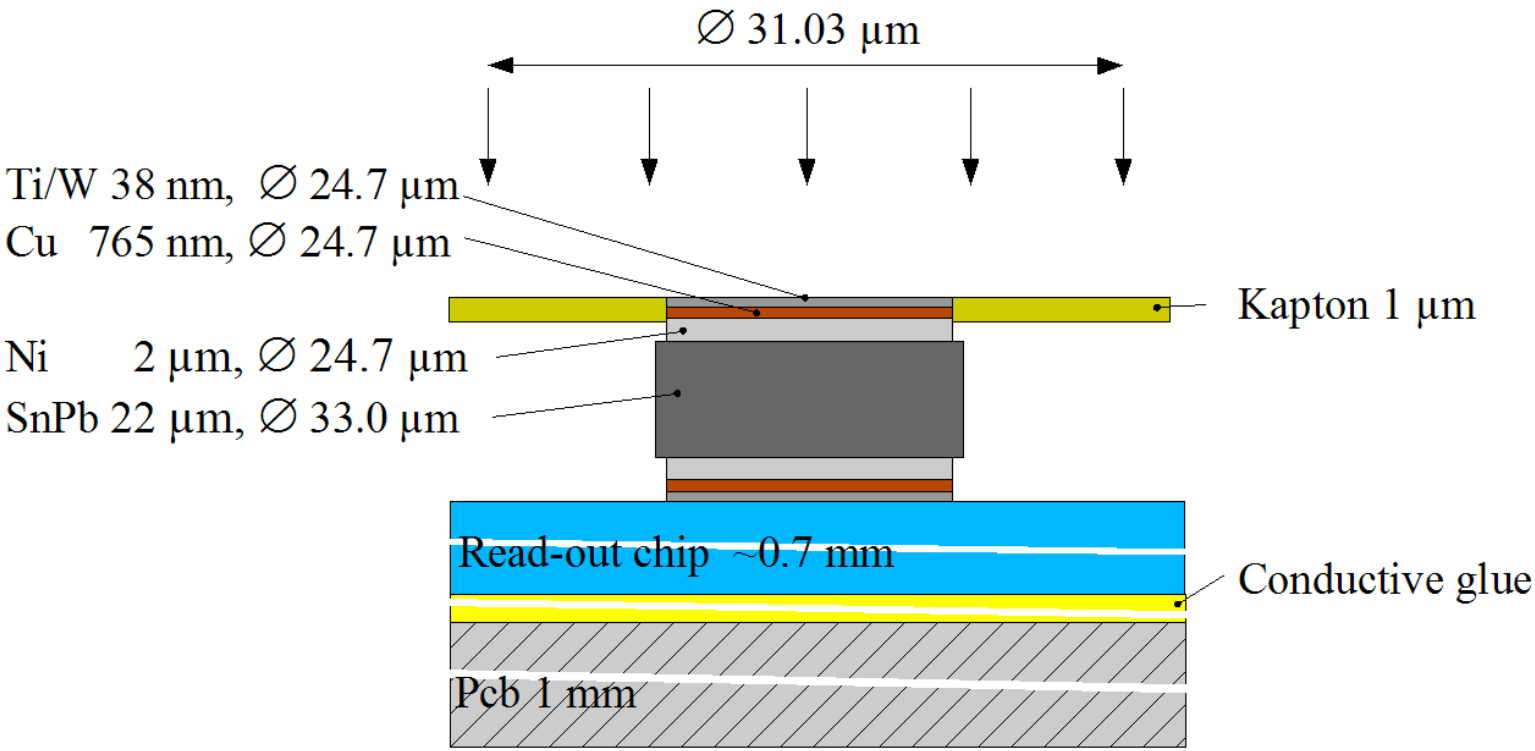


Sn in bump bond 63%

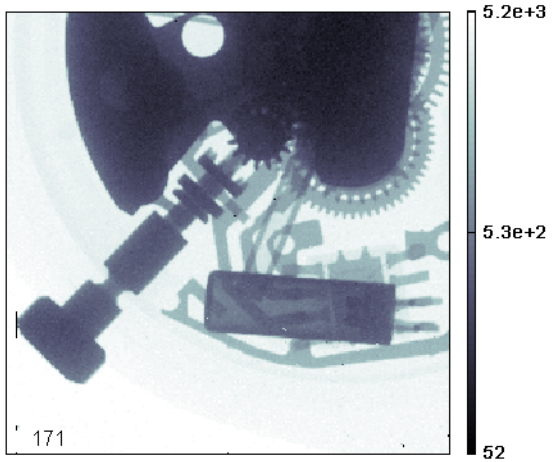
Spectroscopic information – insight into environment

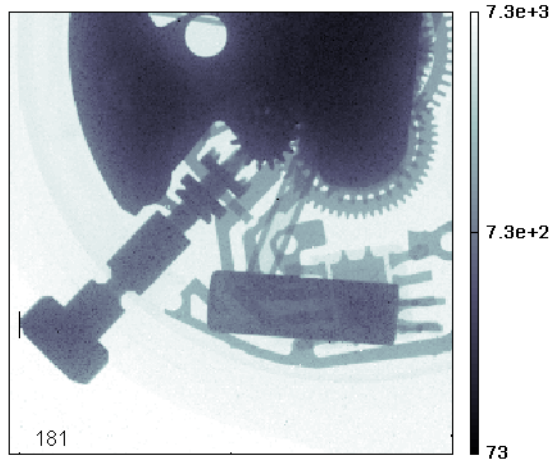
Siefert FK-61-04x12 X-ray tube, W-target, 2.5 mm Al, V_{peak} = 50 kV.

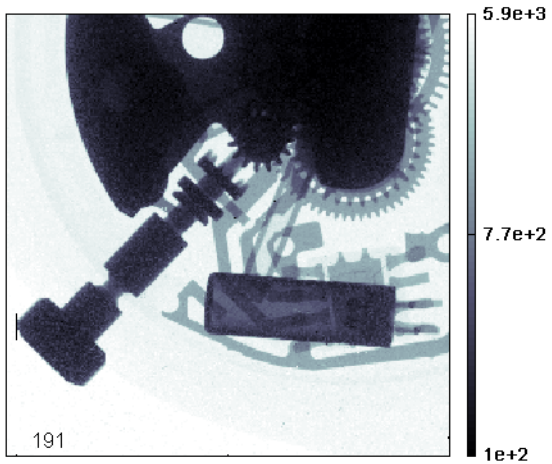
Cross section of a solder bump bond

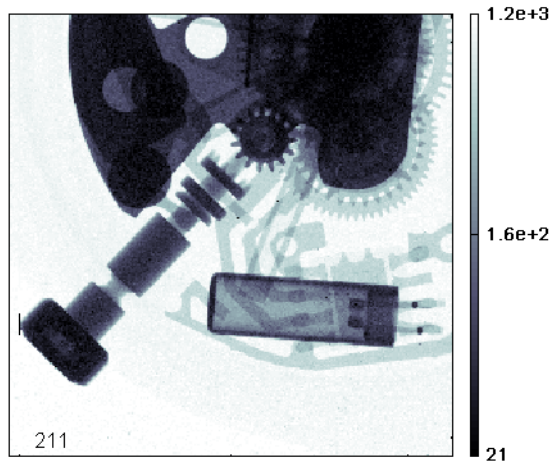


Images of a Swatch using the Energy Window









Medipix2 Experience

- Single photon counting is a reality – see demo
- Noise free imaging possible over a large range of dose rates

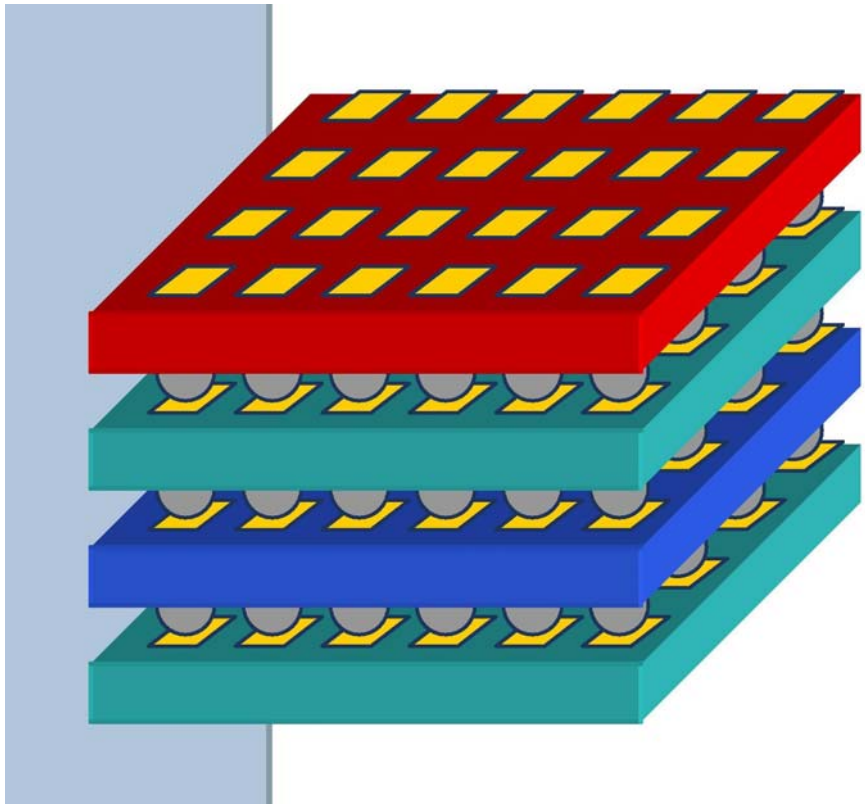
- Spectroscopic behaviour limited by charge sharing between pixels
- Chip only 3-side buttable

Future trends – Medipix3…

- New pixel electronics taking care of charge diffusion – event-by-event clustering
- Higher acquisition and frame rate with dead time free readout – probably using 3-D pixel sensors

- Contiguous tiling of large areas – making using of deep via technology
- More efficient X-ray detection with uniform high-Z sensor material

2-D Tiling concept



Sensor

Interposer

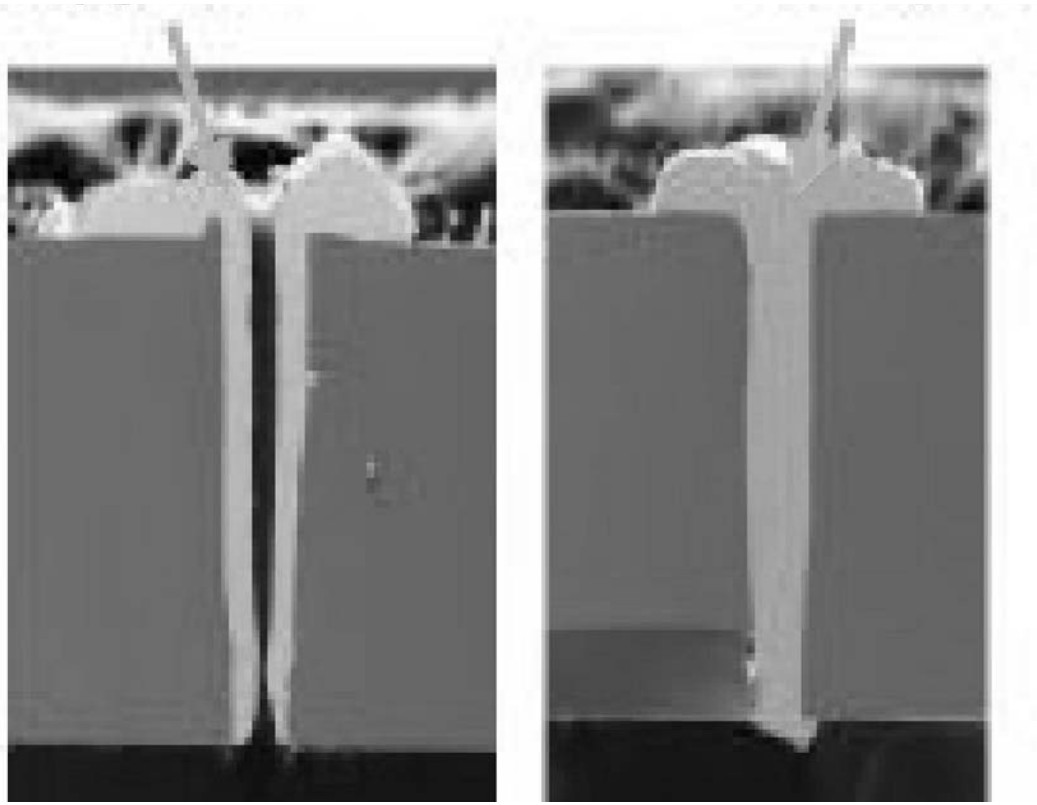
Readout

DSP

IMEC

[J. John, Proceedings of IWorid meeting, Sept. 2003 Riga (next 2 slides)]

Through wafer hole plating

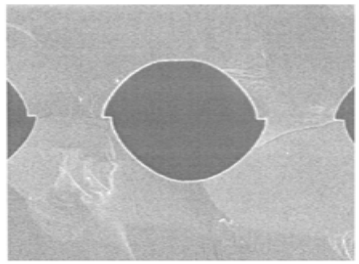


IMEC

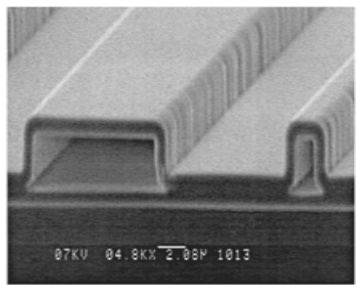
W plugs in Si wafer
NB Post processed wafer T_{max} 400 C

Novel cooling techniques

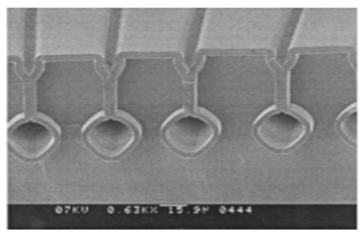
- 3 examples of micro cooling channels
- Must look for solutions which can be used post processing (<400 C)
- Interconnection of channels between chips remains a challenge



(a)



(b)



[J. Meint et al, Journal of Microelectromechanical Systems, Vol. 9 (1), March 2000]

The way ahead…

- Following the evolution of CMOS is unavoidable
- Cost of prototyping becomes a major issue – calls for the formation of a large consortium
- 4 side buttable tiling needs to be developed
- There are promising developments in cooling which may be adopted although a major effort is still required

- Future developments in CMOS promise much for radiation imaging detectors

But for now….

Acknowledgements

- **Fellow members of the Medipix Consortium**
  - www.cern.ch/medipix

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