IFDEPS 2018

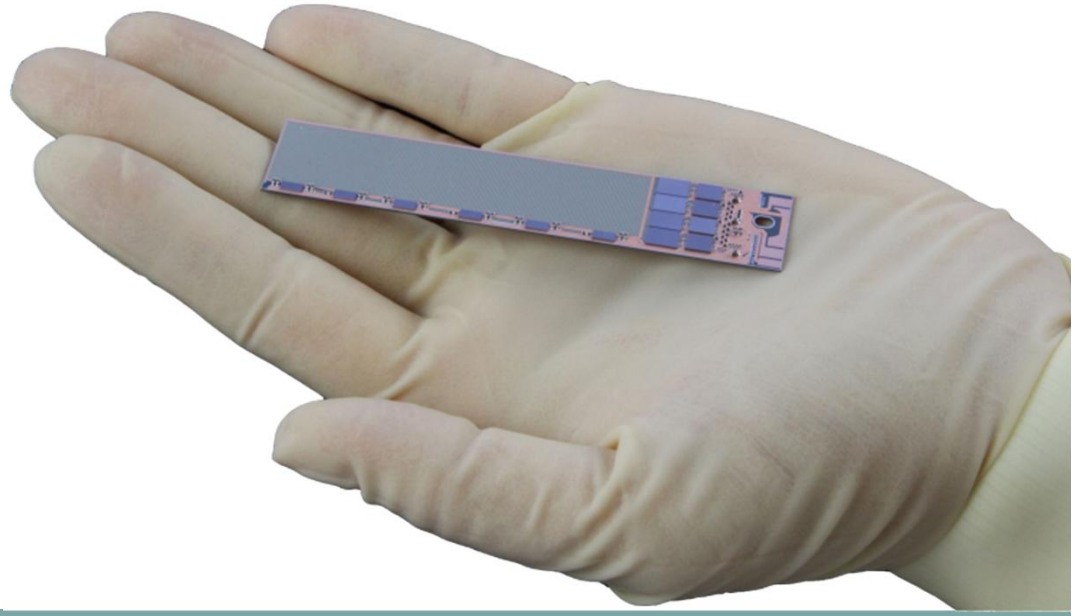
Advanced Multielement and Position Sensitive Energy Dispersive Detectors

# Status, Prospects and Challenges of State-of-the-Art Detector System Integration

Annecy, 12.3.2018

J. Treis[1]

on behalf of the MPG Semiconductor Laboratory



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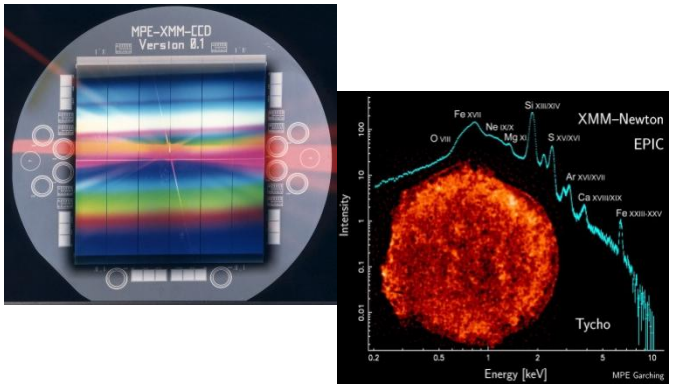
- Introduction
- Detector portfolio
- The Challenges
- The TrueTile concept
- 4SBC modules

# Introduction

"Traditional" target applications:

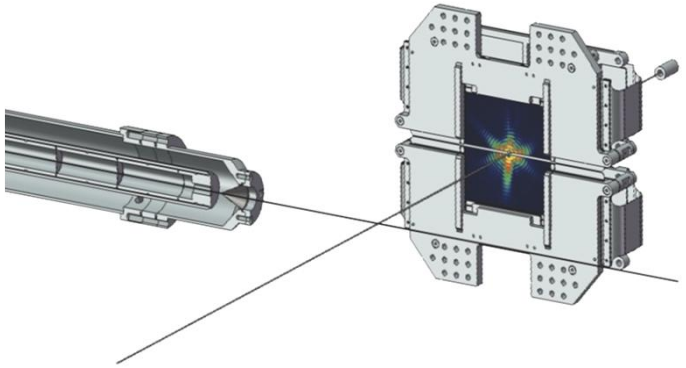
Spectroscopic imaging

- Medium to low energies (15 – 0.1 keV)
- Near Fano-limited spectral resolution
  - Readout noise 1 - 10 e- ENC
- High spectral performance
  - P2B ratios > 5k @ Mn-Kα
  - 100 % fill factor
  - High QE @ Low Energies (60 % @ C-K, 30 % @ B-K)




Diffraction pattern imaging

- Medium to low energies (15 – 0.1 keV)
- Low noise / interpolation
- Single photon counting capability
- High dynamic range
  - Charge handling capacitance 0.8 – 1 x $10^6$ e-
- Operation in vacuum

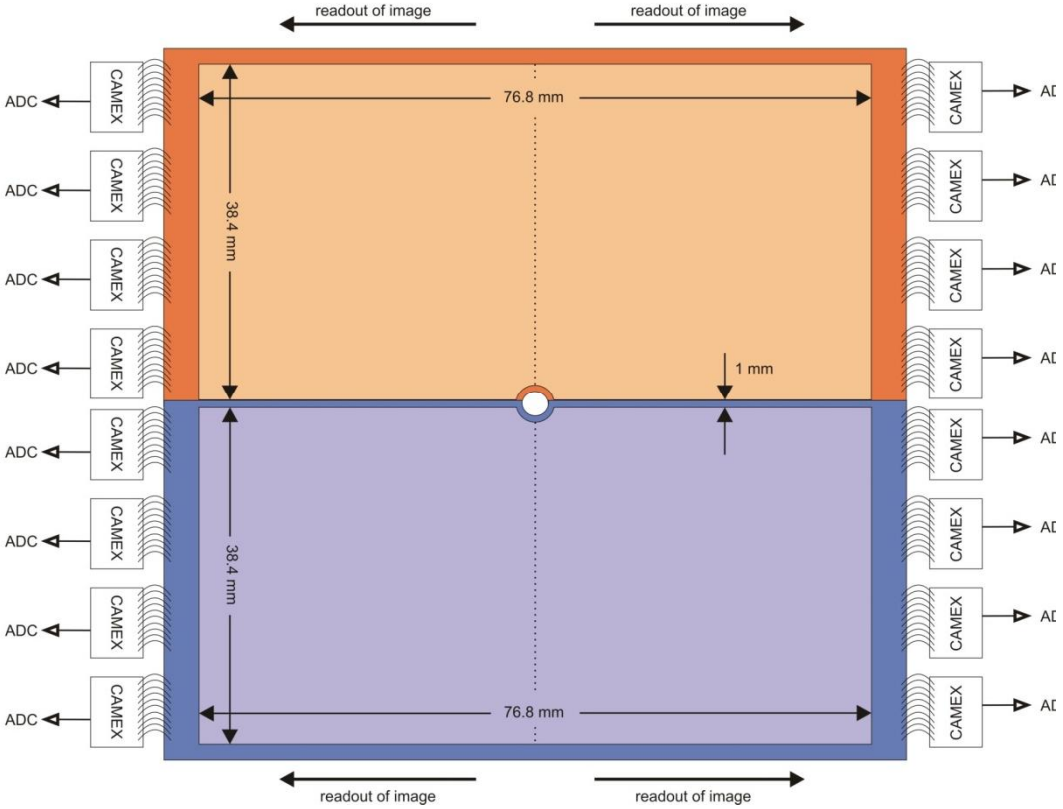


# Introduction

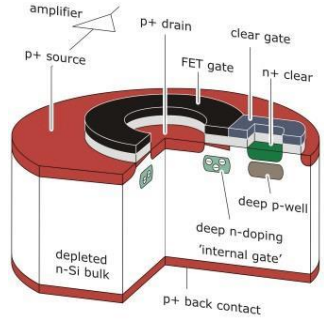
Large area pnCCDs

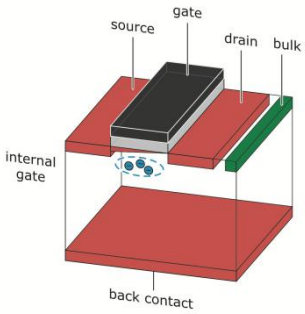
- use at synchrotron radiation facilities (CAMP / LAMP)
- 2 x 1024 x 512 pixels
- area 7.8 x 3.7 $cm^2$ = 29.6 $cm^2$
- 60 $cm^2$ total sensitive area
- pixel size 75 x 75 $\mu m^2$
- 1024 parallel read nodes
- 6 $e^-$ @ 120 fps
- 4k x 4k resolution points

  (@ 6 keV, no pileup)



# Detector portfolio




## Standard DEPFET

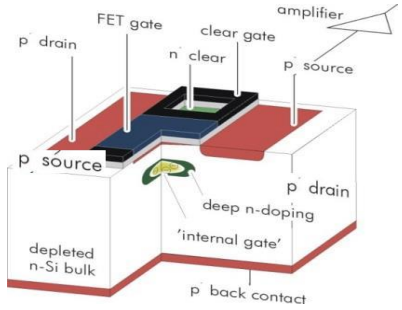
- Sidewards depleted
- Internal gate

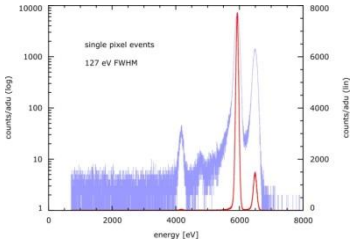
## Circular DEPFET

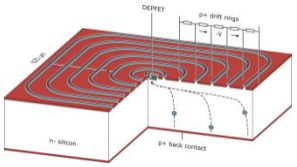
- Large pixels > 75 µm$^2$
- Noise ~ 4 e- ENC
- Efficient filling of area
- Macropixel compatible

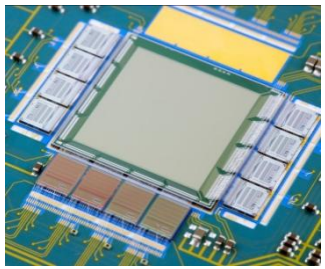
## Linear DEPFET

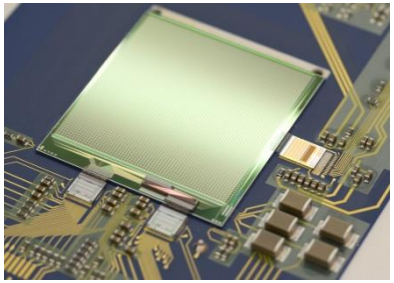
- Small pixels > 25 µm$^2$
- Noise ~2 e- ENC
- High packing density
- Array compatible

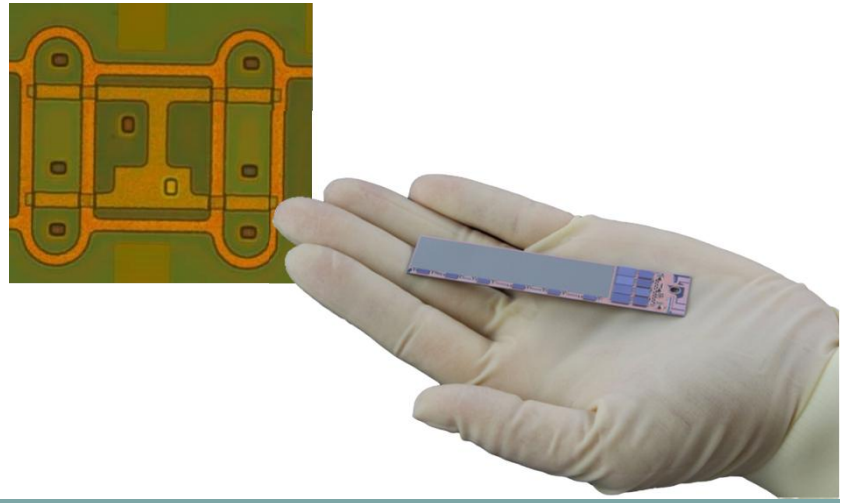


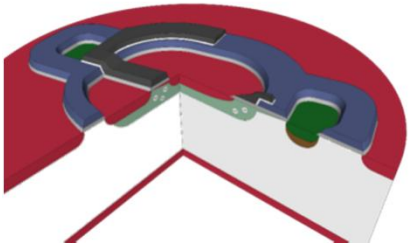





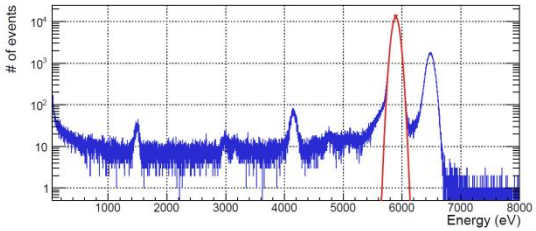


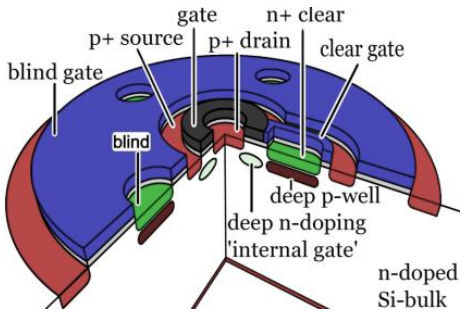
# Detector portfolio



## Semicircular DEPFET

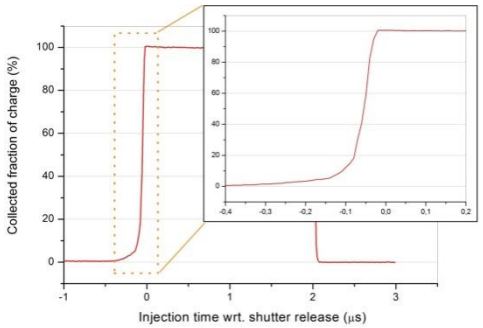
- Combine advantage from linear and circular device
- Large pixels > 150 µm$^2$
- Noise ~ 1.5 e- ENC
- Macropixel compatible

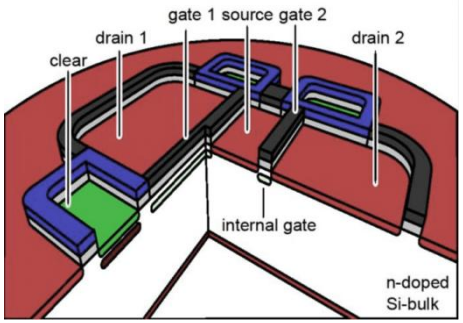



## GPIX DEPFET

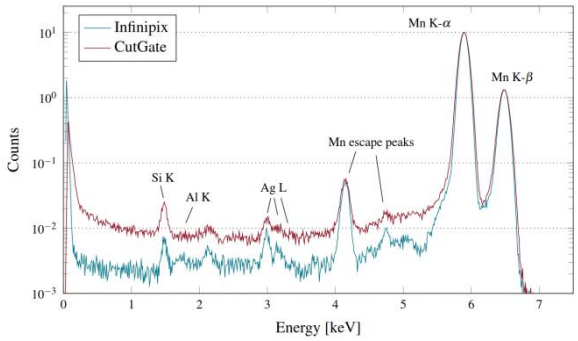
- Add electronic shutter capability
- Overcome rolling-shutter effects
- Precision gating & timing < 100 ns



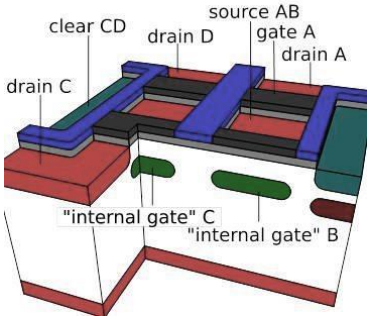




## Infinipix

- Two storage nodes
- Overcome rolling-shutter effects
- Fast timing @ optimal spectral performance
- Array compatible
- Macropixel compatible

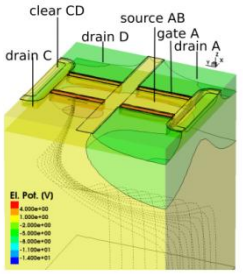


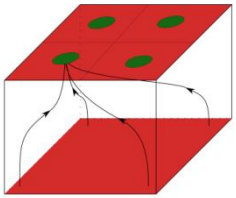
# Detector portfolio

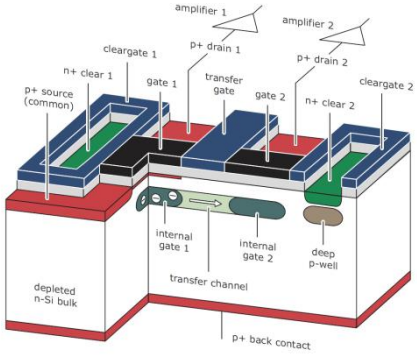



## Quadropix

- 4 storage nodes
- Periodic time slicing
- MicroMovies
- Suppression > 1 ‰
- Time resolution < 100 ns
- Upgrade to Octopix under investigation

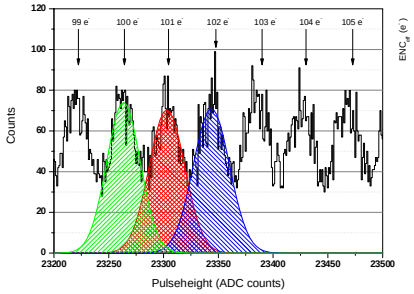


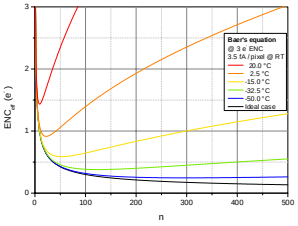



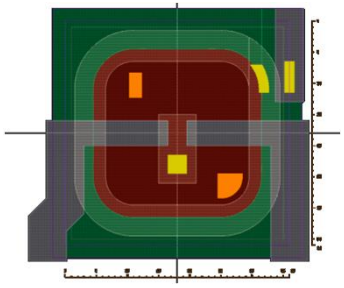



## RNDRpix

- Repetitive non-destructive readout
- Self-Calibrating
- Ultra-low noise
- Incremental / differential imaging

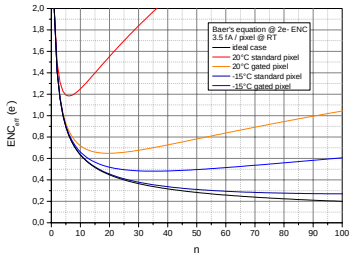


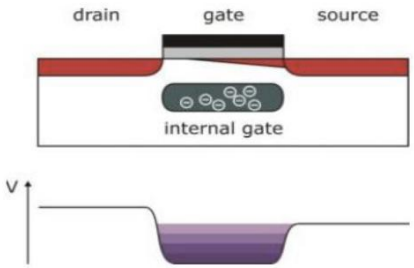



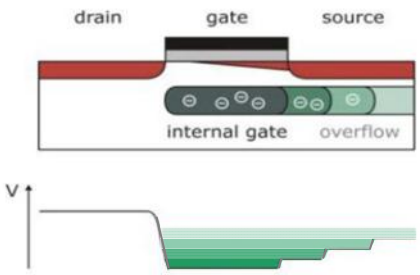
## RNDRpix

- Repetitive non-destructive readout
- Included electronic shutter
- Suppress shaping artifacts
- Incremental / differential imaging



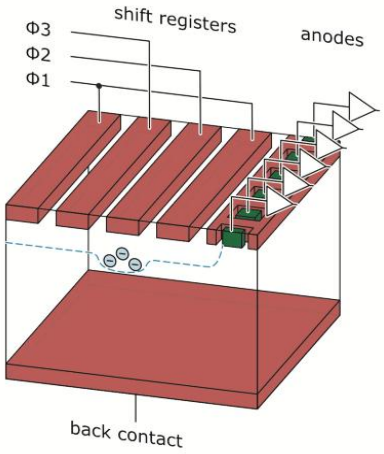
# Detector portfolio



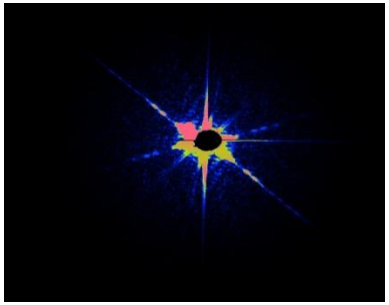

Extended dynamic range:

- Tailor pixel response to experimental requirements
- Use "overflow" regios for internal gate
- Create in-sensor analog signal compression
- Implantatnions and topologic variations

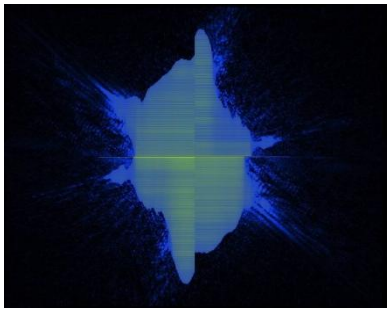



Large CHC modes (pnCCD):

- Enlarged pixel CHC / full well capacity
- Improved imaging capability at high intensities
- Special operation mode

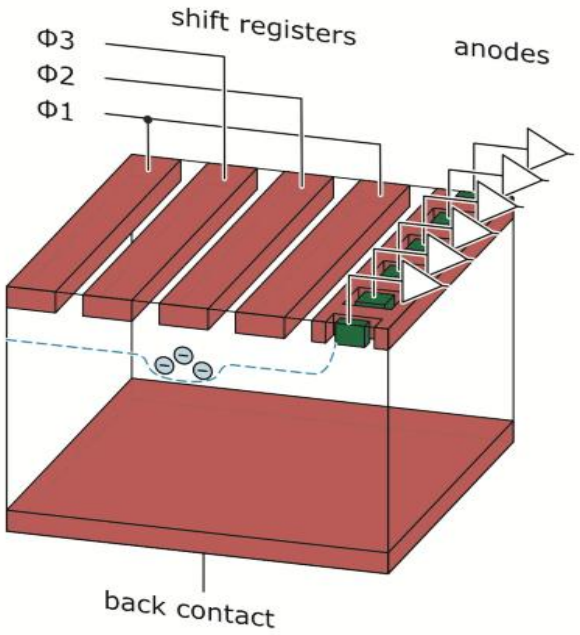


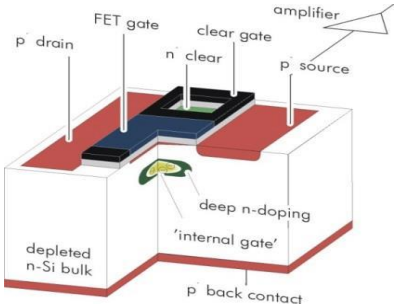
800 ke- dynamic range

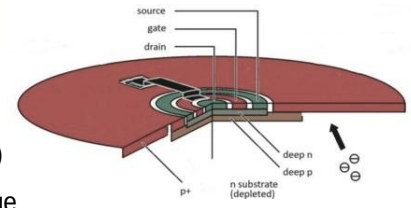


200 ke- dynamic range

# Detector portfolio

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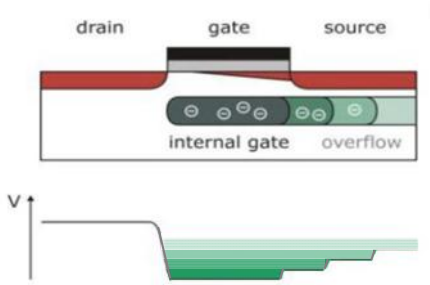


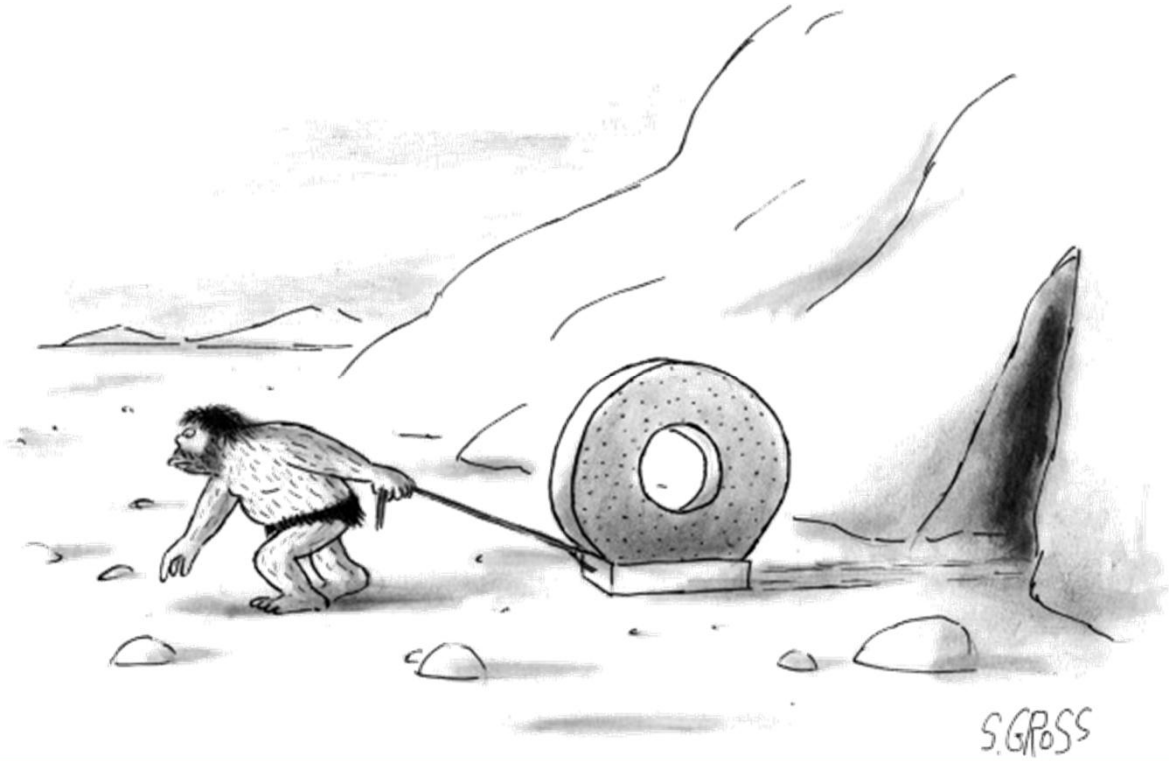

Combination of different conceptual features creates devices with multiple capabilities

CCD2020 devices:

- DEPFET readout w/ all benefits (speed, compression…)
- Narrow guard ring topology for minimized inactive edge
- Virtual pitchadapter / smart binning
- Near room temperature operation

# The challenge

- Make the potential of the sensor devices available
  for state-of-the-art experimental facilities
- Create integration platform suitable for multiple device concepts
- Cope with sophisticated requirements from both facilites and users



# Where to go?

We need:

- Larger areas
- Higher framerates
- Maintain good resolution

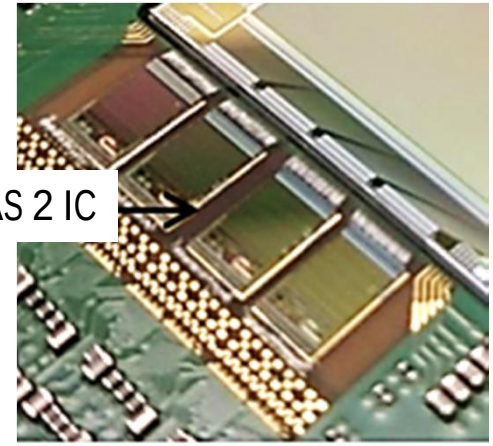
Secondary virtues:

- Low Power
- Higher degree of modularity
- Maintenance friendly

4 main challenges:

- Sensor & front end electronics
- Backend & data acquisition
- Supply and bias
- Thermal management

# Sensor & Front End Electronics



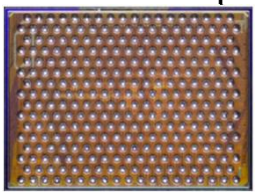

- AMS 0.35µ technology
- 64 channels
- Trapezoidal filter
- Integrated sequencer
- Analog serialization
- Min. shaping time ~ 0.5 µs
- Noise ~ 1 e- ENC

**DCDB** (Drain Current Digitizer)
Analog front-end

Amplification and digitization of DEPFET signals.

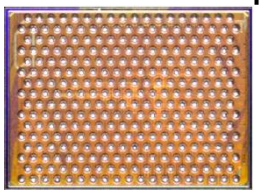
§ 256 input channels
§ 8-bit ADC per channel
§ 92 ns sampling time
§ new version w/ 50ns sampling time under test
§ UMC 180 nm
§ Noise limit ~

**DHP** (Data Handling Processor)
First data compression



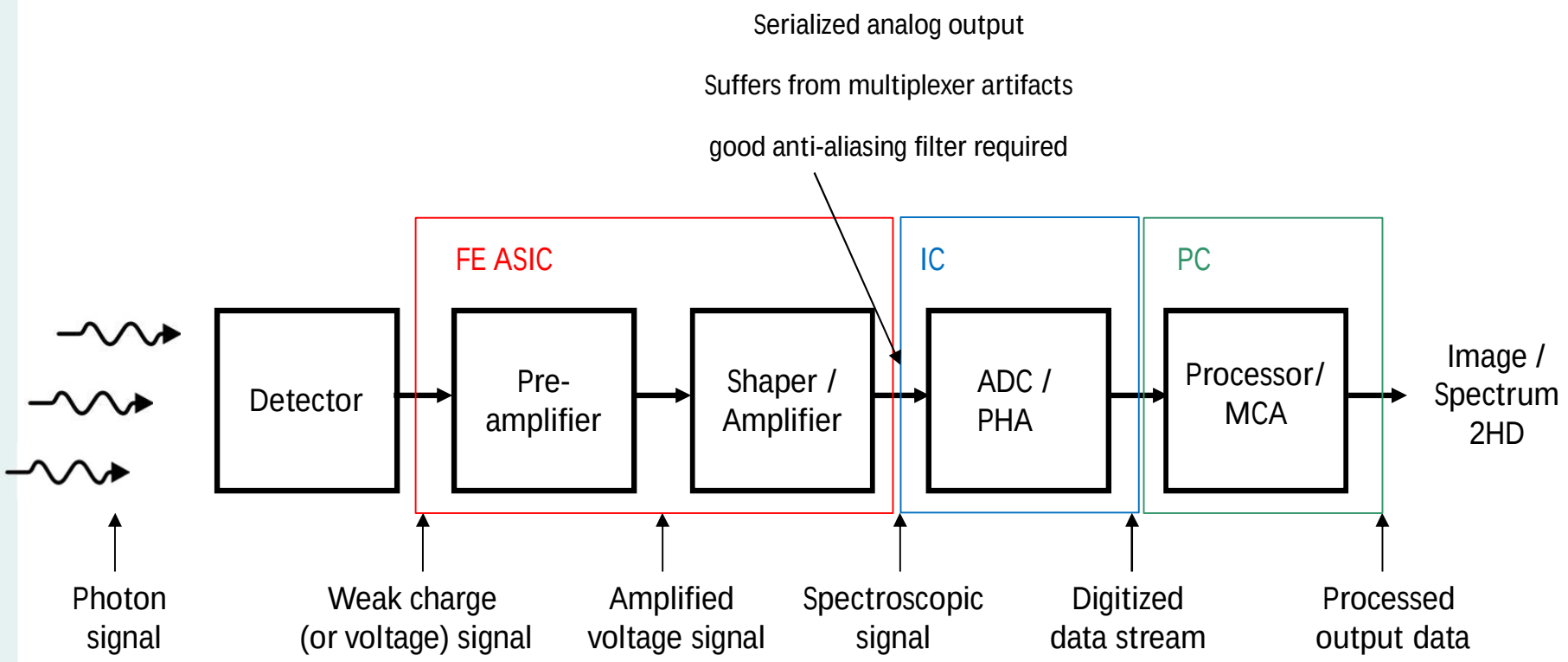
IBM CMOS 90 nm (TSMC 65 nm)
§ Size 4.0 ´ 3.2 mm$^2$
§ Stores raw data and pedestals
§ CM and pedestal correction
§ Data reduction (zero suppression)
§ Timing and trigger control
§ Drives fast data link

**DMC** (DEPFET Movie Chip)
First data compression



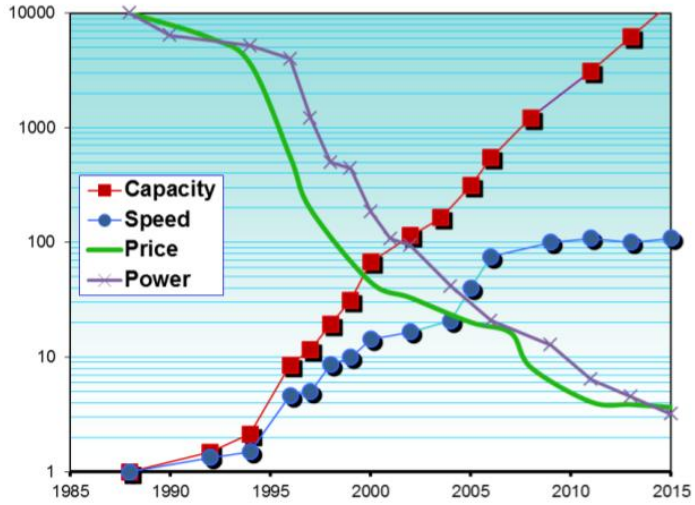
TSMC 40nm
§ Size 4.0 ´ 3.2 mm$^2$
§ Stores unprocessed image data
§ Sufficient memory for 100 frames
§ No data reduction)
§ Timing and trigger control
§ Drives 8 slow data link

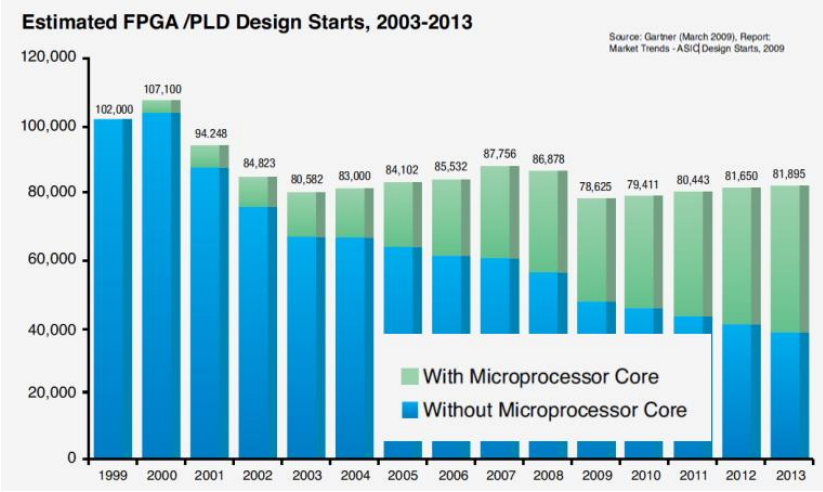
# DAQ Backend: The analog way



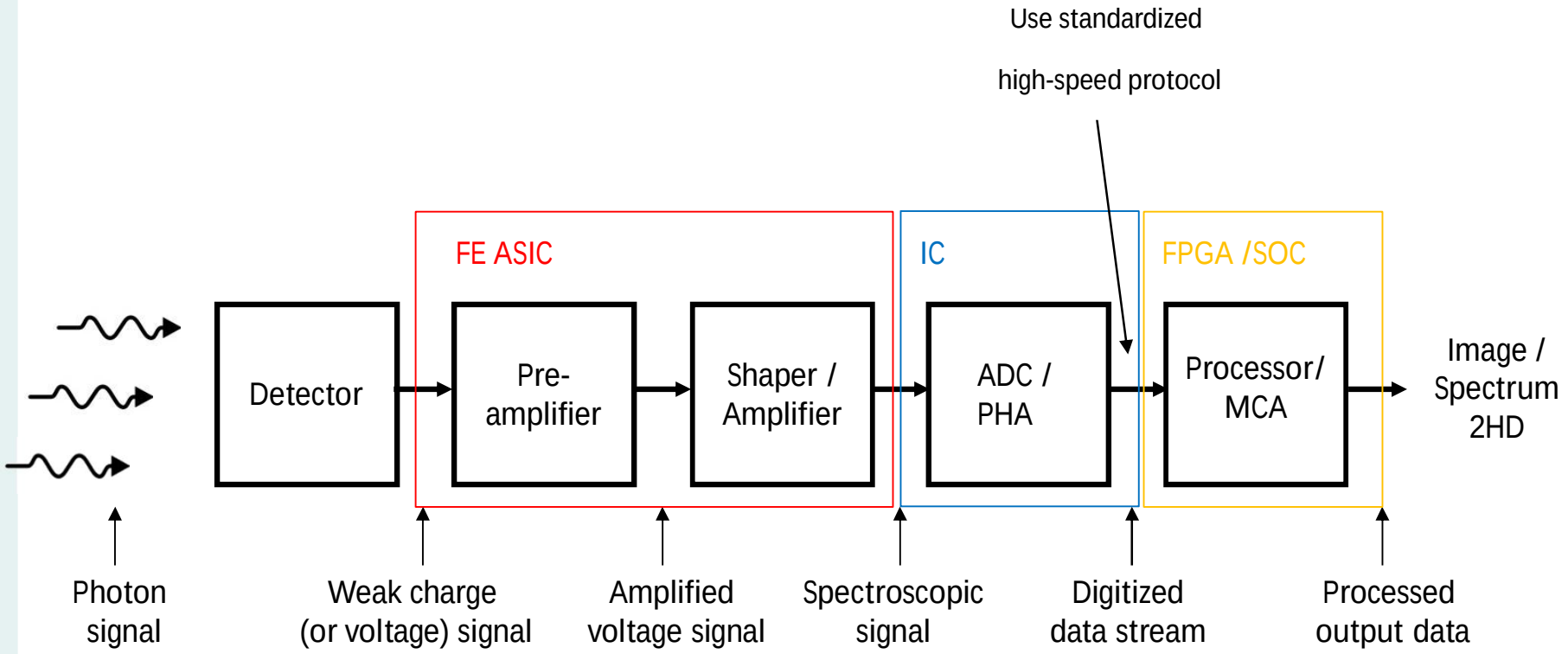
# DAQ Backend

- FPGA based solutions:
  - Available FPGA resources and speed keep growing
  - System-on-a-Chip solutions increasingly find application
  - Flexible platform for both Data preprocessing and de-centralized instrument control
  - Included resources for high speed data transmission
  - Ready-made IP(!)

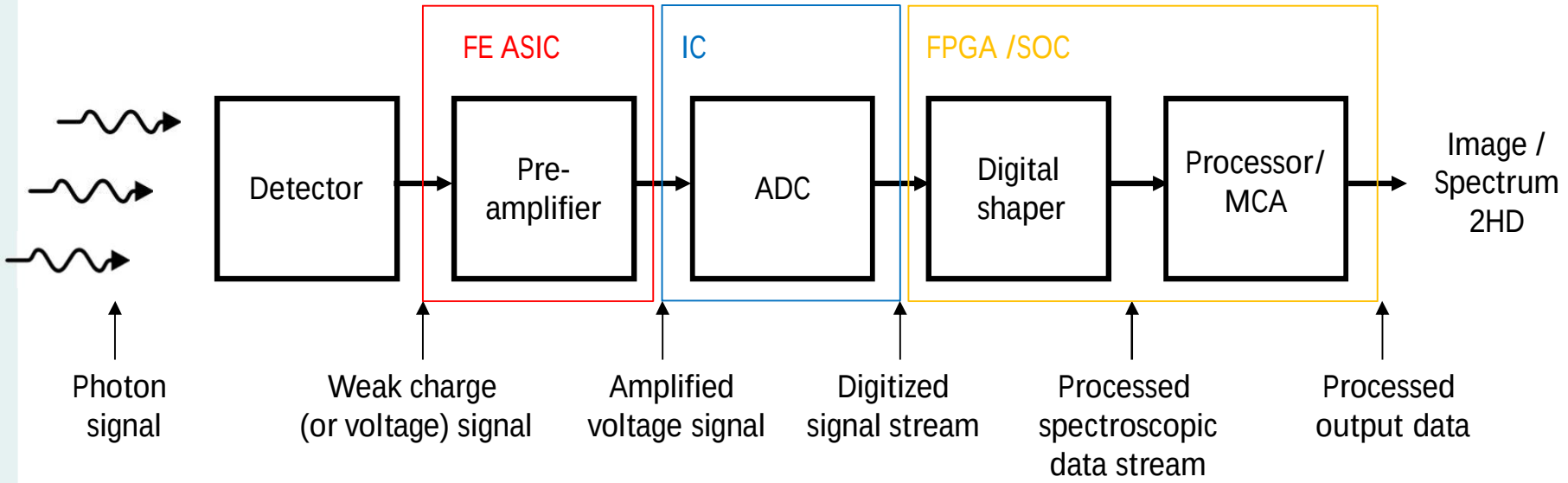


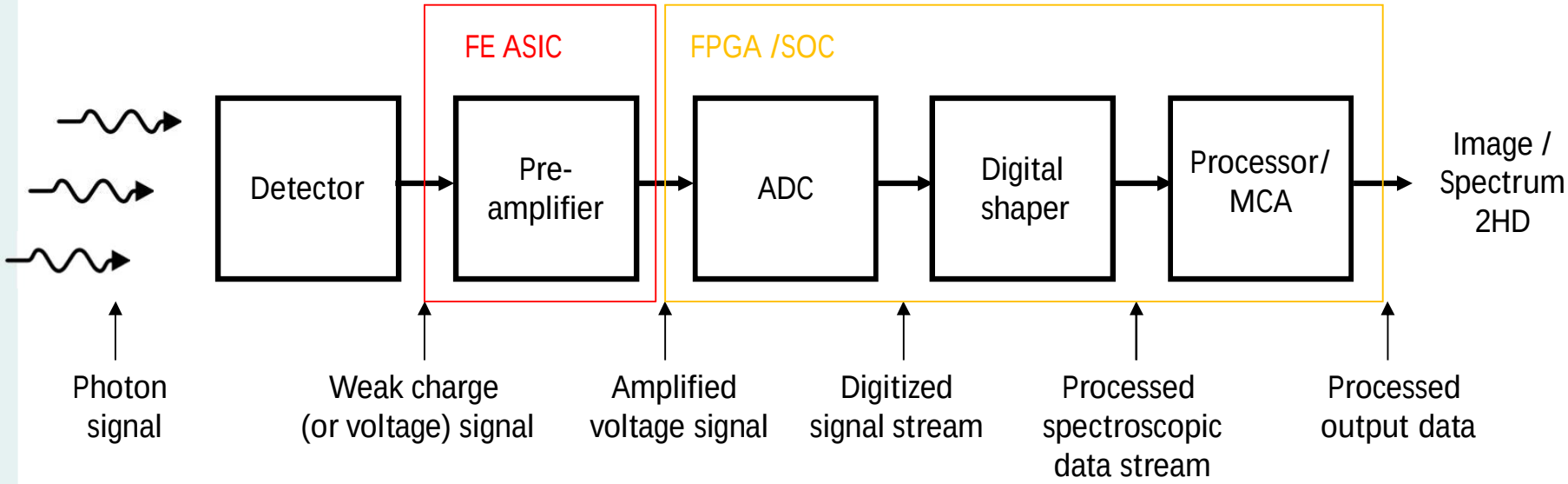
# DAQ Backend


Use standardized
high-speed protocol
FE ASIC
IC
FPGA /SOC
Detector
Pre-
amplifier
Shaper /
Amplifier
ADC /
PHA
Processor/
MCA
Image /
Spectrum
2HD
Photon
signal
Weak charge
(or voltage) signal
Amplified
voltage signal
Spectroscopic
signal
Digitized
data stream
Processed
output data

# DAQ Backend


FE ASIC
IC
FPGA /SOC
Detector
Pre-
amplifier
ADC
Digital
shaper
Processor/
MCA
Image /
Spectrum
2HD
Photon
signal
Weak charge
(or voltage) signal
Amplified
voltage signal
Digitized
signal stream
Processed
spectroscopic
data stream
Processed
output data

# DAQ Backend


FE ASIC
FPGA /SOC
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Processor/
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Image /
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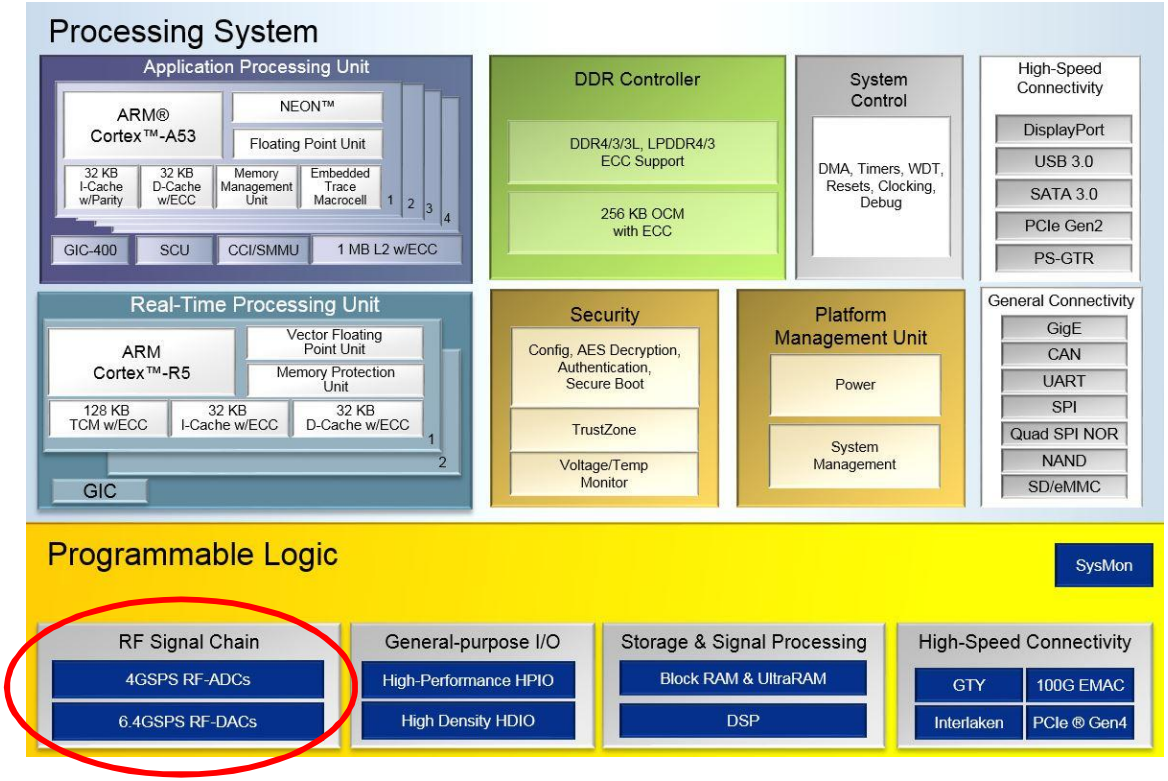
2HD
Photon
signal
Weak charge
(or voltage) signal
Amplified
voltage signal
Digitized
signal stream
Processed
spectroscopic
data stream
Processed
output data

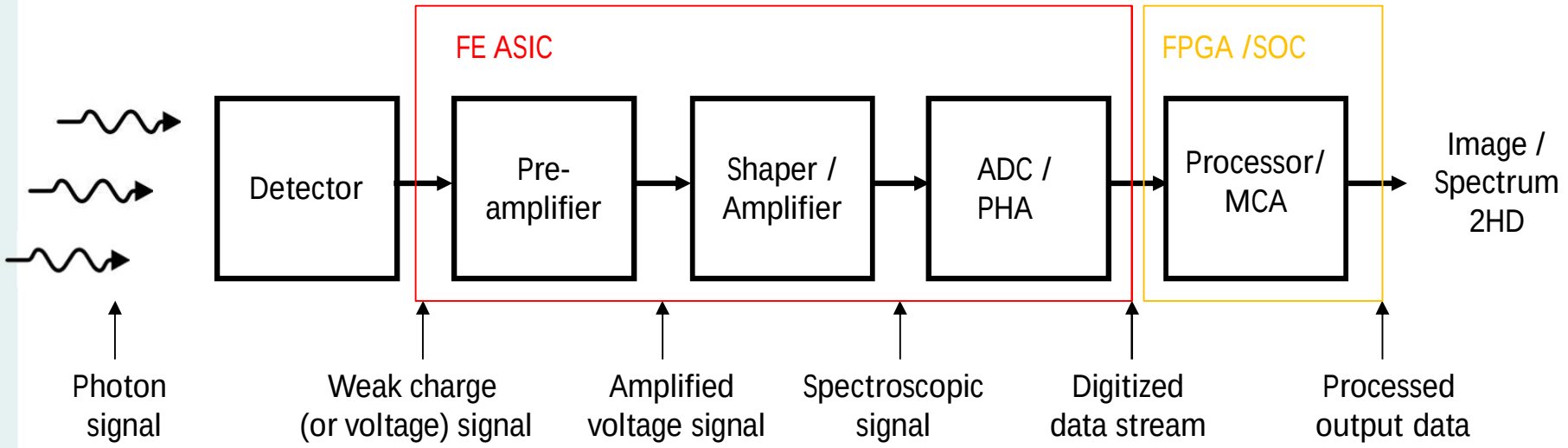
# DAQ Backend




Xilinx Zynq UltraScale+ RF SoC

"Kids today with all their technology."

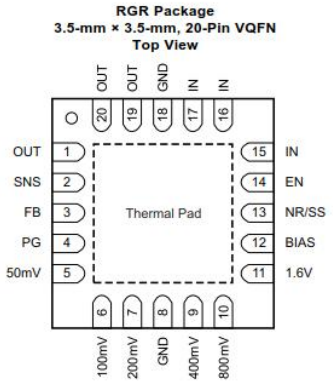
# DAQ backend: The digital way



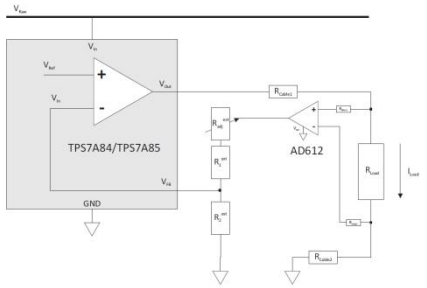
# Supply & bias

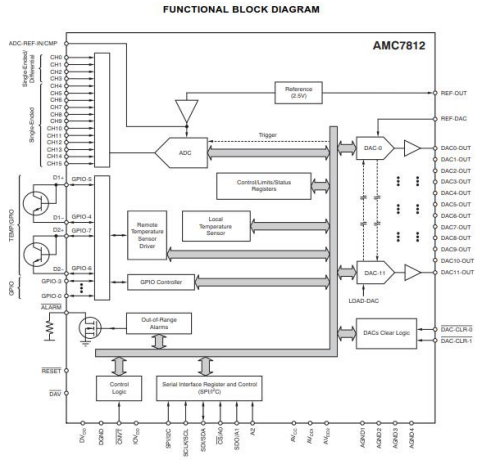
Challenge:

- Larger number of readout ICs
- More advanced IC technology
- Potentially higher bandwidth
  - Higher current draw @ lower voltages
- High packing density / small allowable trace width budget
- Finite trace resistance (technology-depending)
  - Growing need of small, decentralized low-noise regulators
  - Point-of-load (area)
  - Sensing (Hi- and potentially also Lo- side)
  - End of the paradigmatic multi-channel power supply rack
- Implement housekeeping circuitry
- Efficient prereg circuitry using compact DC/DC converters

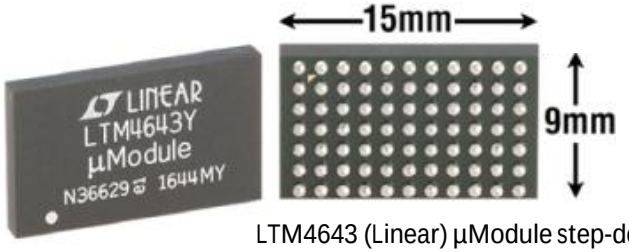



TPS7A85 (TI)
4 A 0.8 V – 5V, 4 $uV_{rms}$ LDO




AMC7812 (TI)
DACs,ADCs and Digital I/Os




LTM4643 (Linear) µModule step-down converter
12 (!) A, 0.6 V – 3.3 V, 89% efficiency

# Thermal management

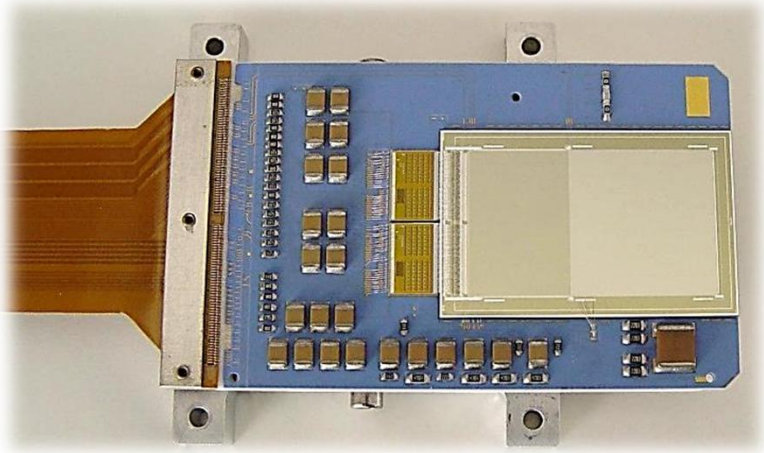
Task:

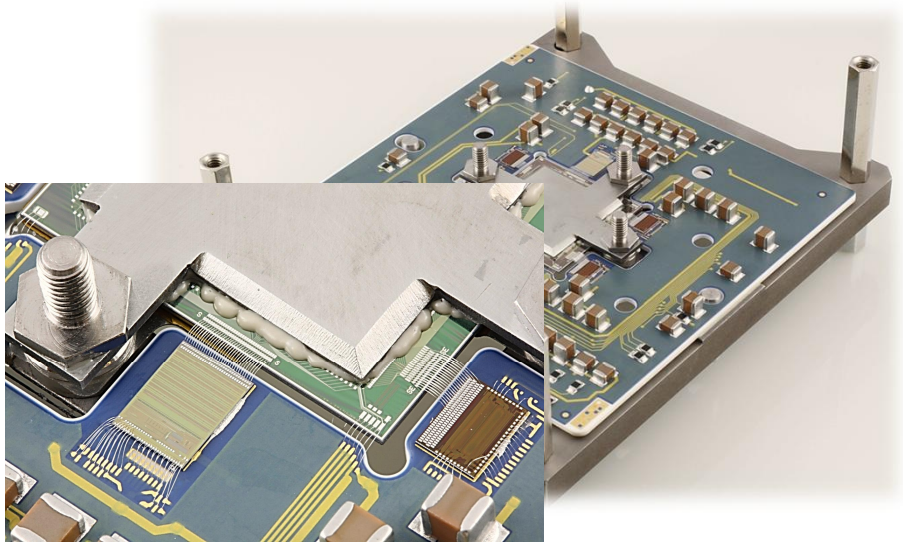
- Removal of waste heat
- Thermal stabilization of sensor and FE electronics

Challenge:

- In vacuum
- Larger number of readout ICs
- Higher readout IC power
- More Sensor readout power
    - More waste heat
- Reduce thermal mass / overall heat coapacitance
- Reduce instrument downtime

    - Thermal decoupling of Sensor and FEE?
    - Low temperature compatibility of FEE?

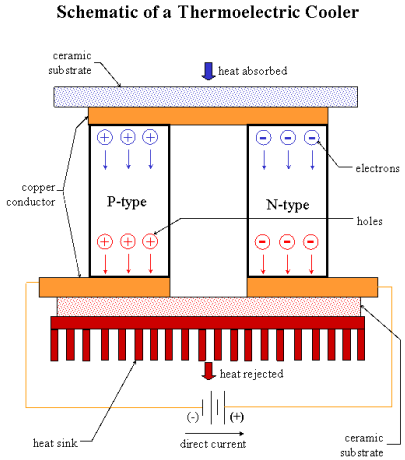




# Thermal management

Options:

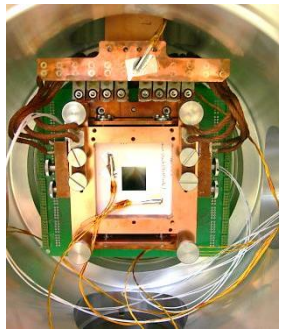
- Cryocooler
  - Limited cooling power
  - Limited regulation capacities
- Peltier cooler
  - Low efficiency
  - Limited temperature range
  - Temperature difference power dependent
  - Huge waste heat generation
- Chiller
  - Limited temperature range
  - Defined by cooling medium
  - Pipework installation required

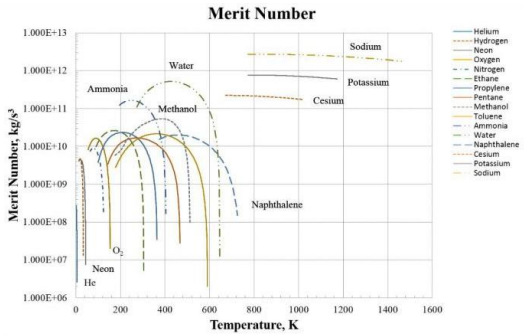

# Thermal management

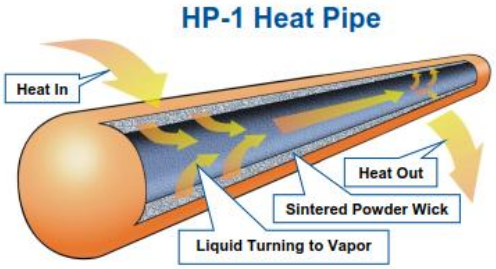
Options:

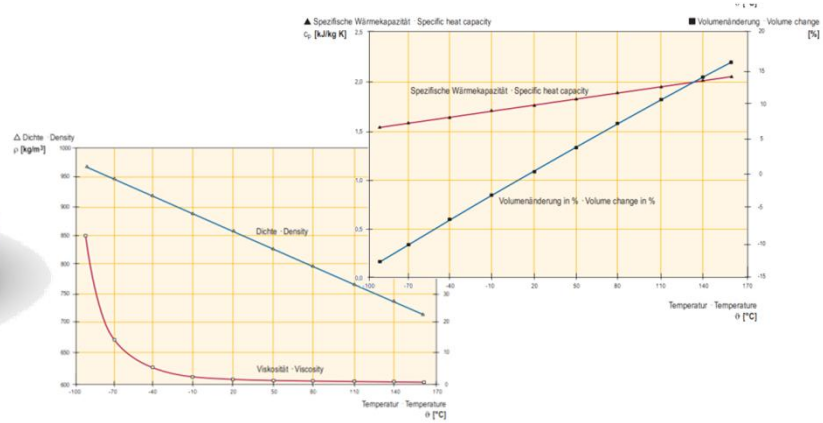
- Solids
  - Cooldown dynamics defined by smallest heat conductivity
  - Huge thermal mass
  - Huge actual mass
- Heatpipes
  - Fast
  - Limited temperature range
  - Limited efficiency for low temperatures
- Cooling medium
  - Cooldown dynamics defined by mass flow
  - Liquid / gas-tight pipeworks
  - Wide range of media
  - Varying efficiency



$$N_l = \frac{\rho_l \sigma \lambda}{\mu_l}$$

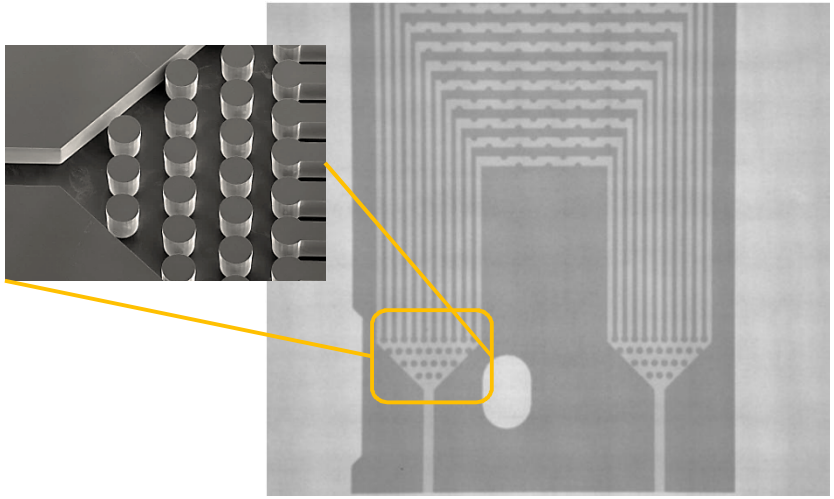


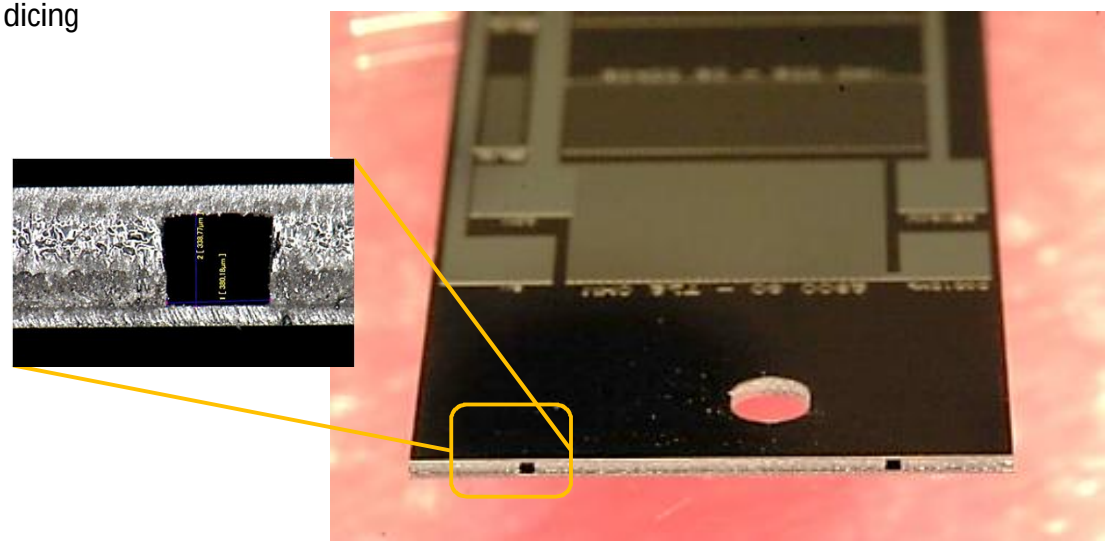



# Thermal management

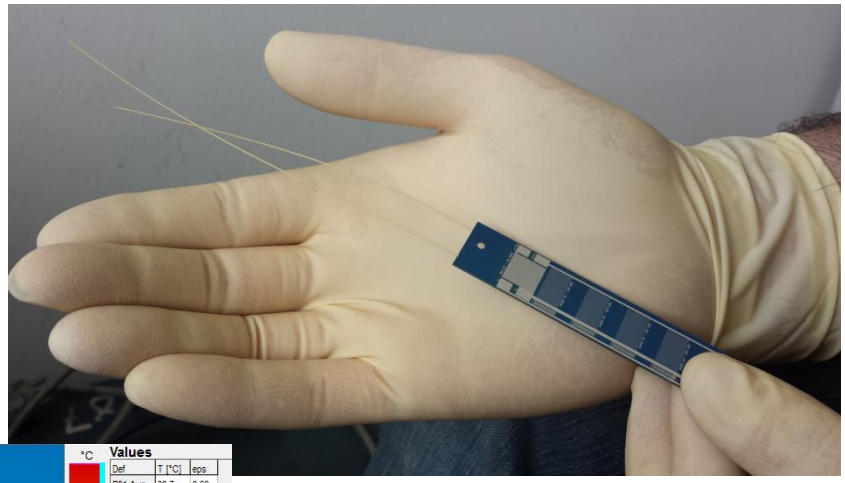
- Microchannel cooler (MCC):
  - Plasma-etched channels in silicon wafer
  - Wafer bonded to lid wafer to hermetically seal channels
  - Thinning / tailoring of thickness according to requirements
  - Channel design according to heat load distribution
  - Wafer can be processed like a normal wafer / lithography steps
  - Access to channels exposed during dicing





# Thermal management

- Microchannel cooler (MCC):
  - Extremely low thermal mass
  - Extremely fast cooldown times
  - Robust against deformations / vibrations over wide range of pressure
  - Optimum CTE match for Silicon



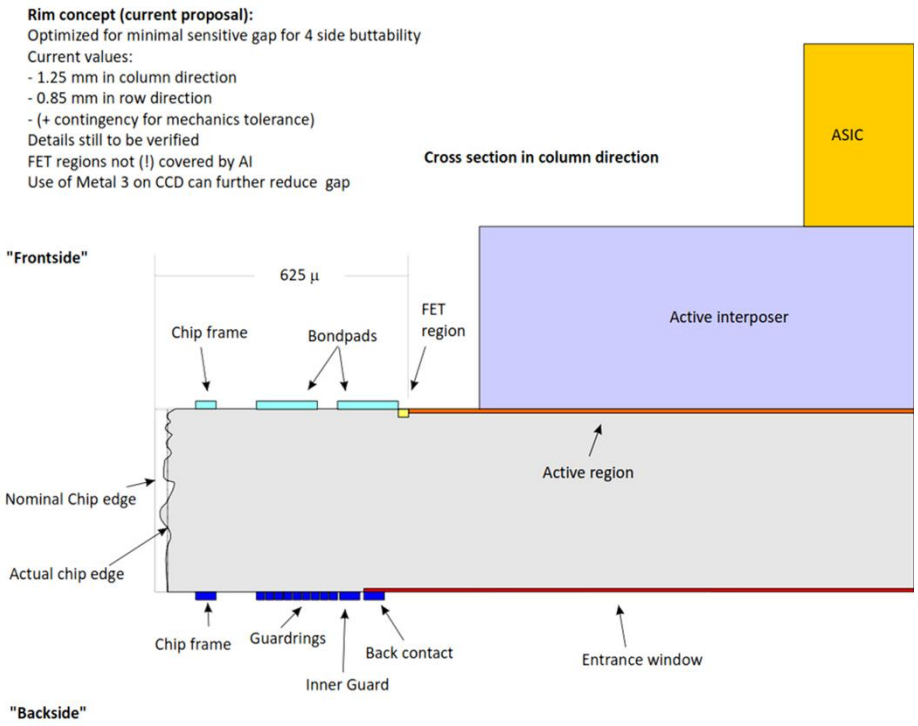

# TrueTile module concept

TrueTile concept:

- 4-side buttable sensor modules with minimal sensitivity gap
- 4 main ingredients:
  - Make guardring structures as narrow as possible for small sensitivity gap
  - Use Active Interposer (AI) unit to host
    - sensor
    - readout ASICS
    - supplementary drivers
    - passive circuitry
  - Accommodate all biasing and backend circuits within AI / Sensor envelope
  - Maximally modular approach

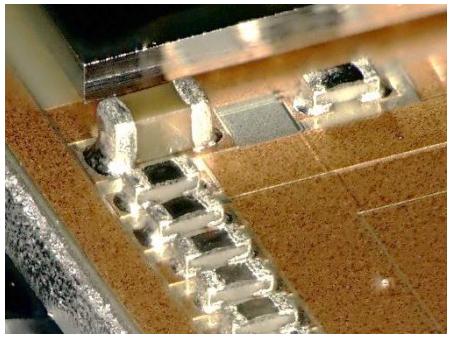
Device independent

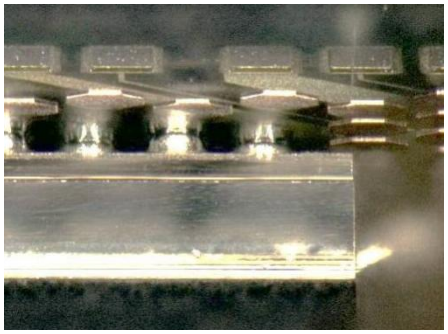
- Platform approach
- Can be adapted to different device topologies
- Very similar backend systems
- Can be inserted in case

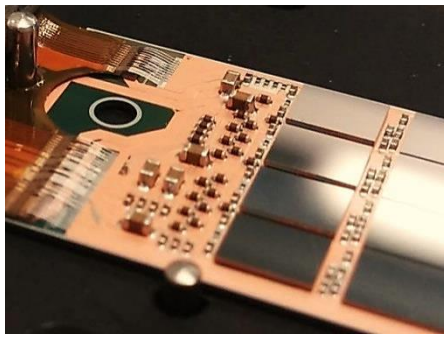


# Learn from HEP: From ASM to AI

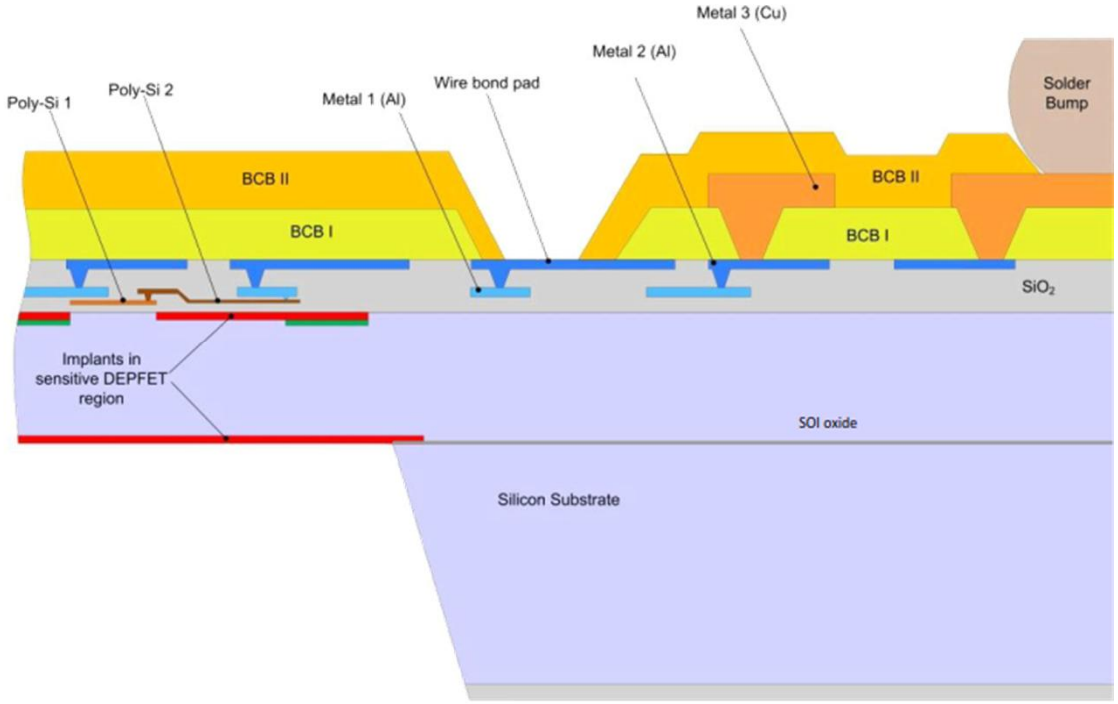
- All-Silicon-Module (ASM):
  - Sensor die includes regions for
    - Front-End-Electronics
    - Passives
    - Signal / Power traces
    - Bond-/Solderpads to periphery
  - "Passive" balcony regions
  - No additional support structure





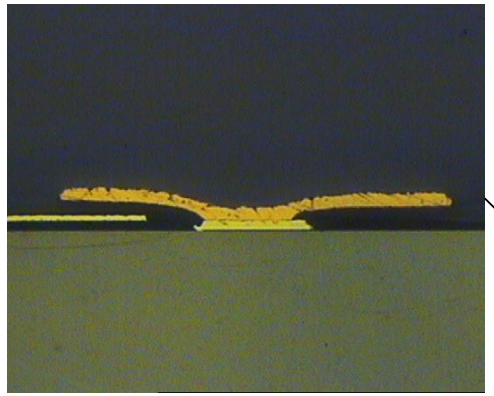


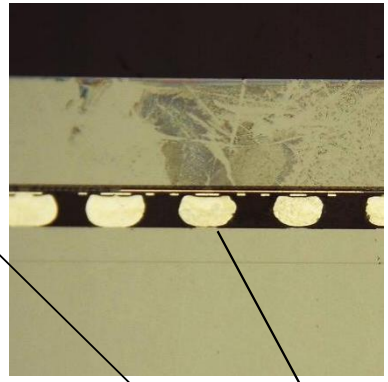
SuperBelle ASM on SOI wafer
w/ thinned sensor region

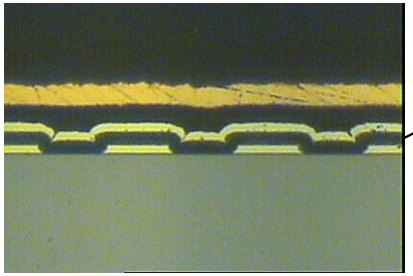


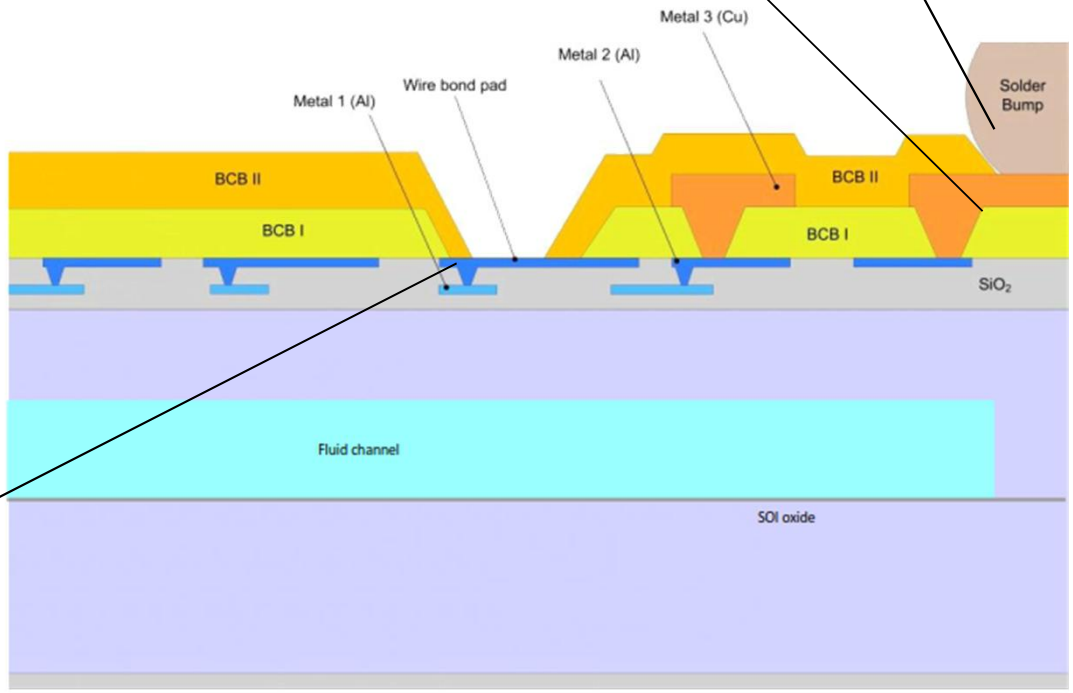
# Active Interposer

- Active Interposer (AI):
  - Silicon interposer based on SOI:
    - Matchmaker / Pitchadapter to sensor die
    - Carrier for FE ASICs and passives
    - Carrier for peripheral connector
    - Substrate for power / signal trace system
    - Container for SOI based MCC
  - Separated from sensor substrate
  - Interface to support mechanics
  - Fine-pitch trace system (lithography level)
  - µBump bond pads for FEE
  - Optimum CTE match to sensor

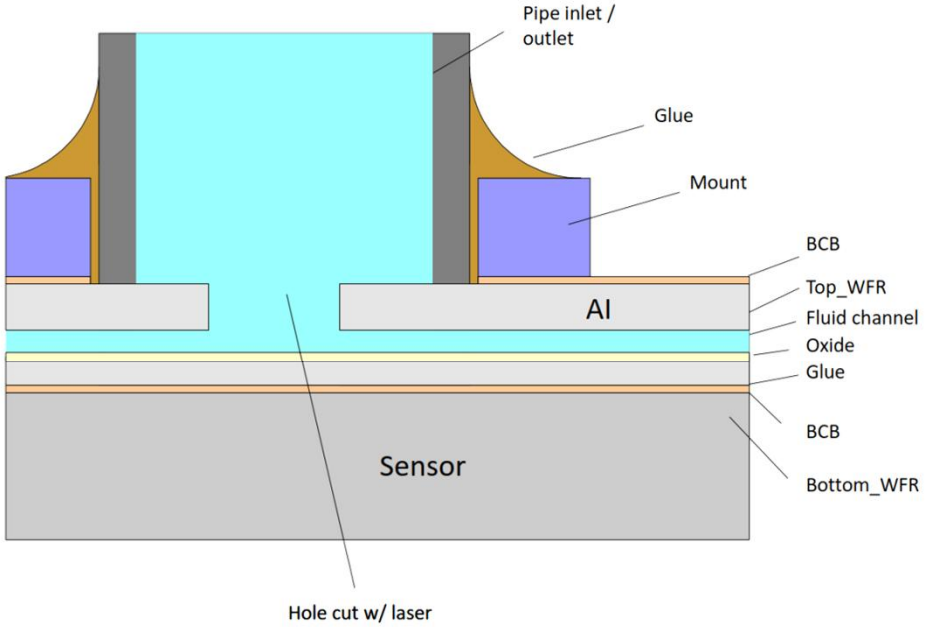


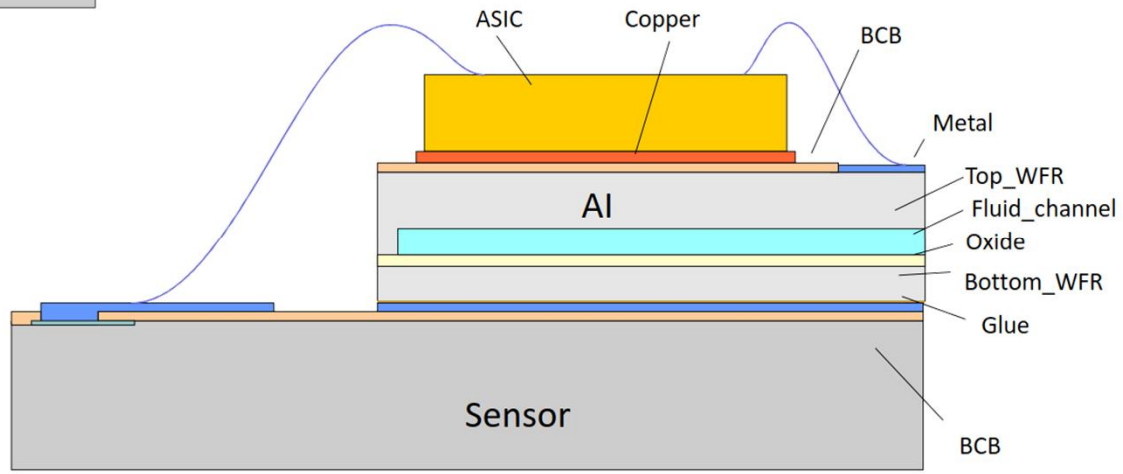






# Active Interposer

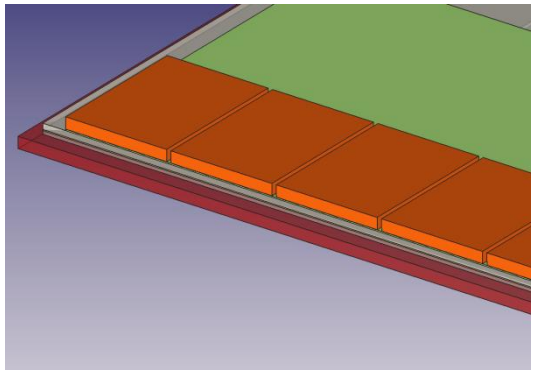


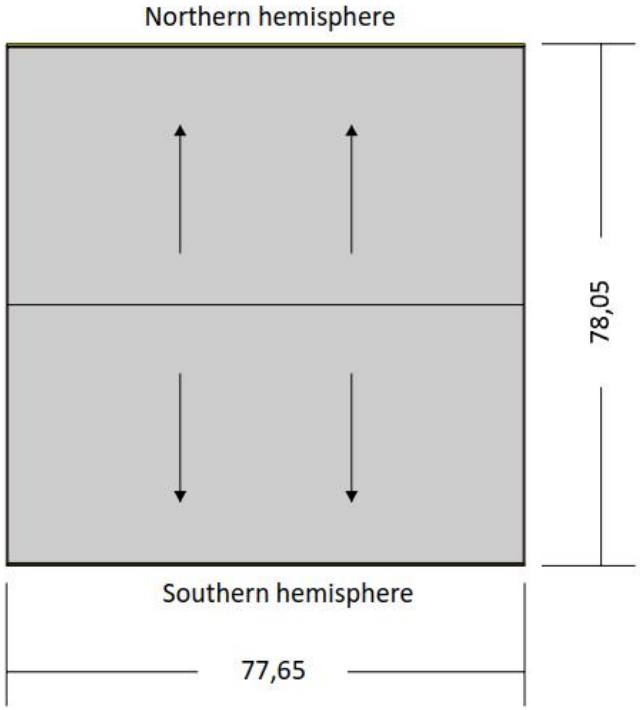

Active Interposer (AI) approach

# Pathfinder: 4SBC

- Pathfinder device architecture:
  - "Conventional" pnCCD
  - Standard mode (no frame store) suitable for synchronous operation
  - Split frame / column parallel readout for optimized framerate
  - 1 MPixel array with 75 x 75 mm$^2$ pixels, sensitive area 76.8 x 76.8 mm$^2$
  - 2 x 1024 JFET (north edge and south edge) readout nodes read in parallel
  - Readout: 2 x 16 x 64 channels VERITAS II IC cores

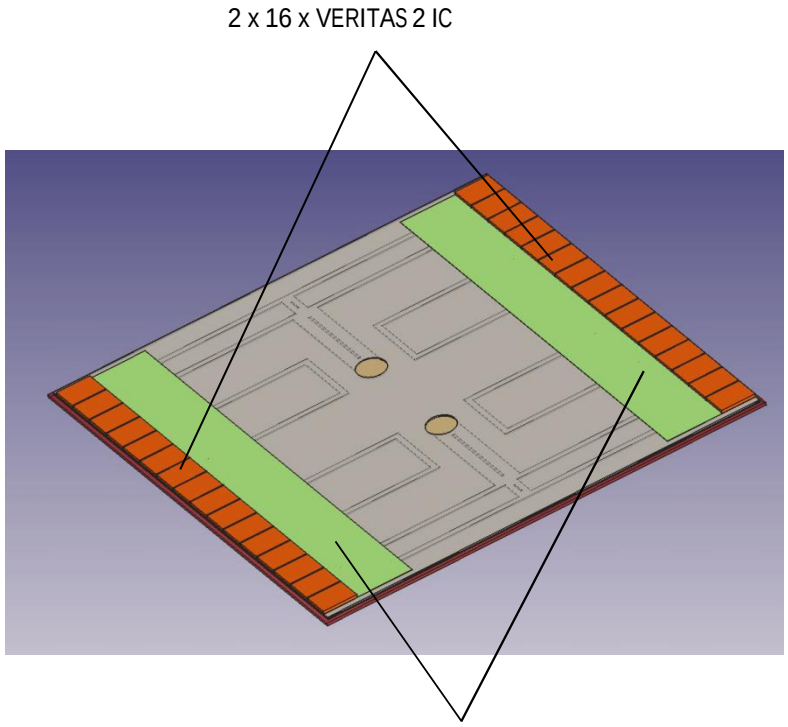


1024 x 1024 pixels
75 x 75 µm$^2$
Sensitive area 76.8 x 76.8 mm$^2$
Standard mode, split frame, column-parallel pnCCD



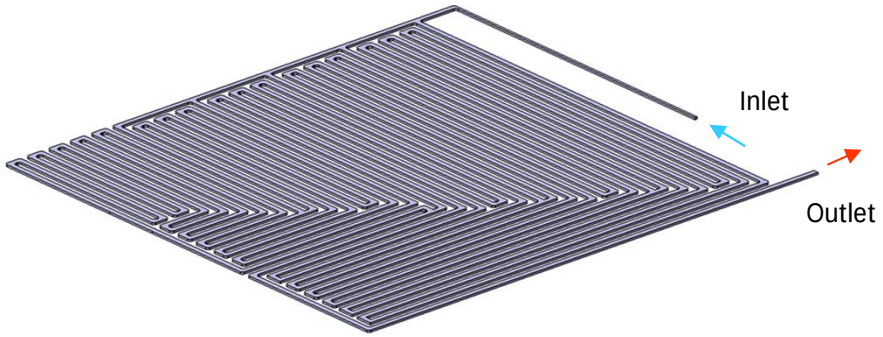
# Data / framerate

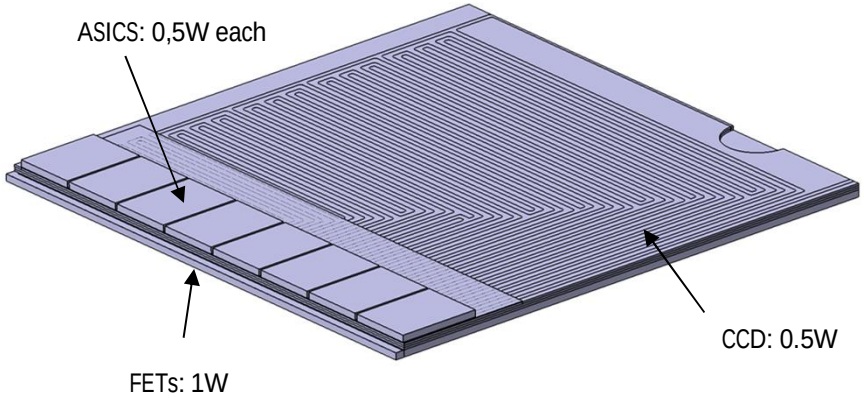
- Conservative estimate:
  - JFET readout nodes w/ VERITAS II IC
  - Readout timing 2 - 4 ms / row @ < 4 e- ENC
  - Split frame: 512 rows
  - Framerate ~ 500 Hz – 1kHz
  - Digitization w/ 14 bit
  - Raw unprocessed data rate ~ 1.1 GB / s
- Reduce data volume by:
  - Data compression (on-module)
  - Applying "Zero-suppression" algorithms
    - Sensor specific corections (common mode etc.)
    - Dynamic noise and threshold determination
    - Hit detection / Cluster recognition
  - Compression factor depends on ocupancy / settings
  - Module-individual on accordingly powerful FPGA

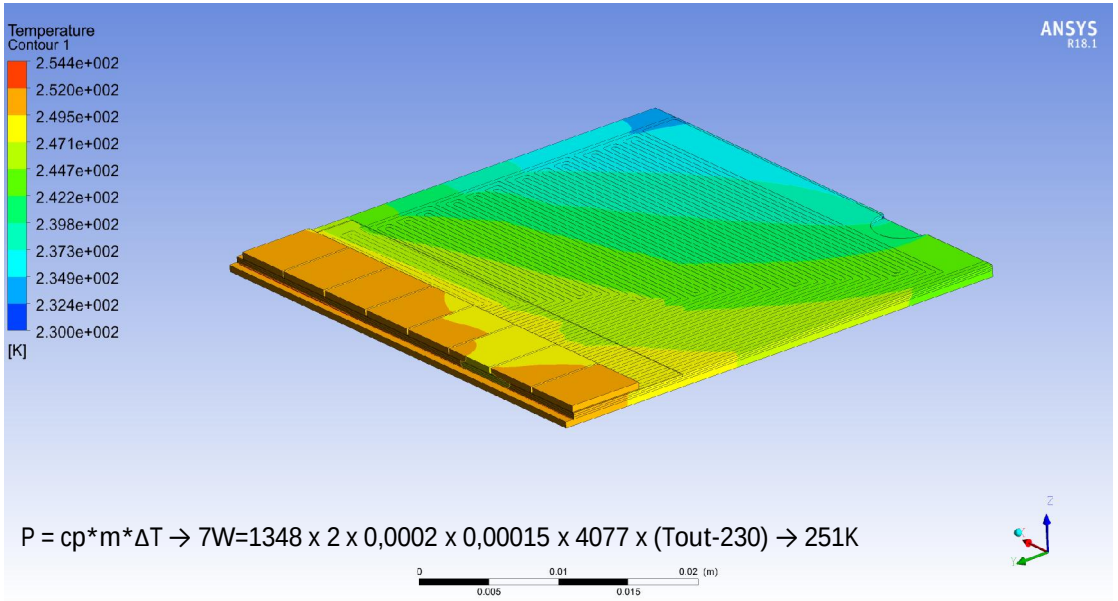



- What if...?:
  - DCD / DMC / DHPT system
  - Readout timing 100 ns ms / row @ > 100 e- ENC
  - Framerate 80 kHz / 10 kHz
  - Digitization w/ 8 bit

# Design & performance of MCC



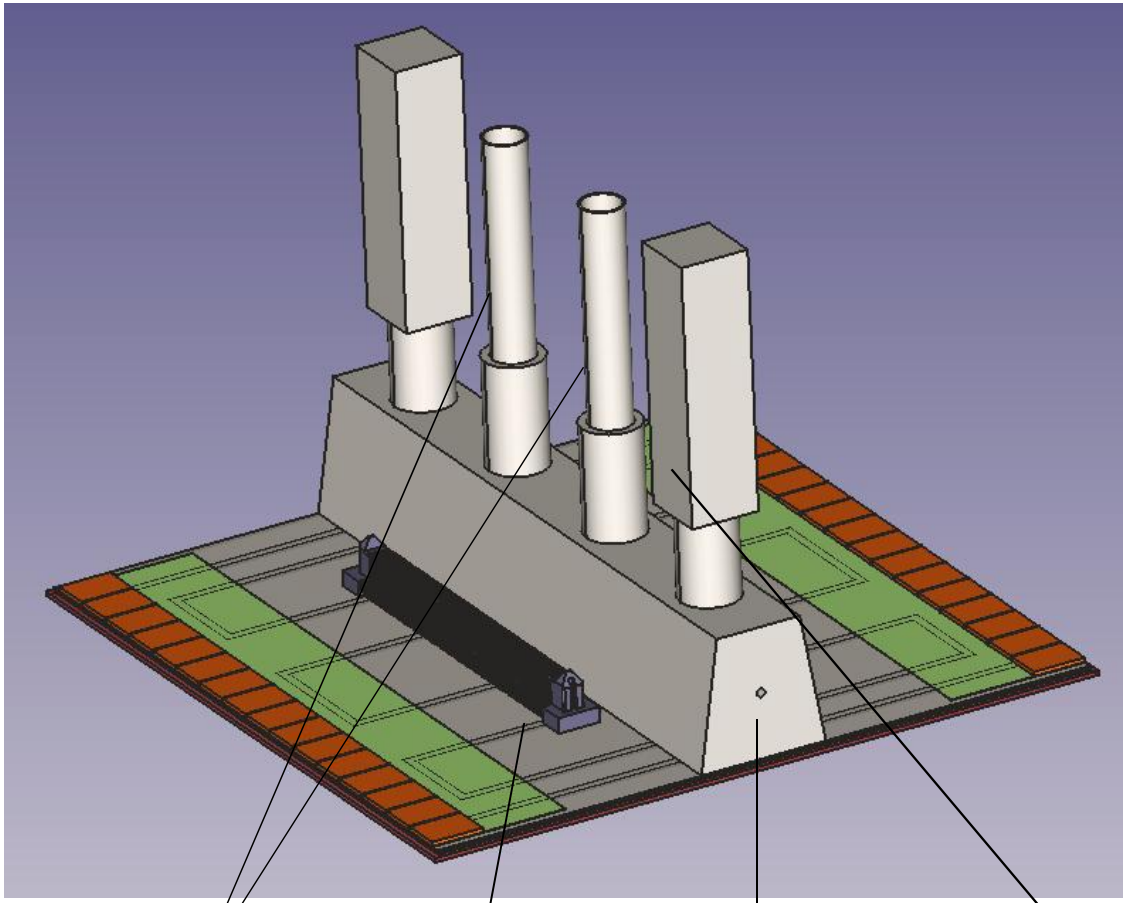

Temperature gradient on device ~ 15°

$T_{out}$ of fluid= 246K
ΔP=3 bar

Design and simulation by
Miguel Angel Villarejo
IFIC Valencia

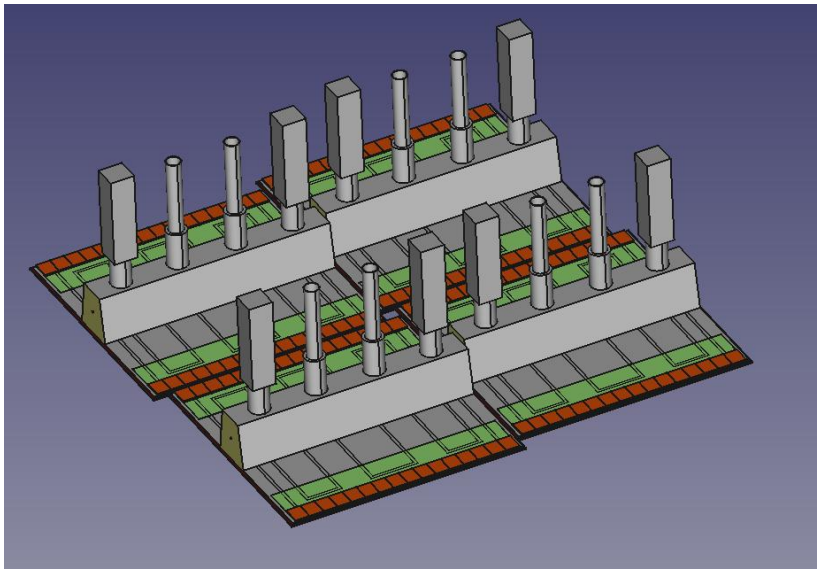
# Mechanical & thermal Interfaces

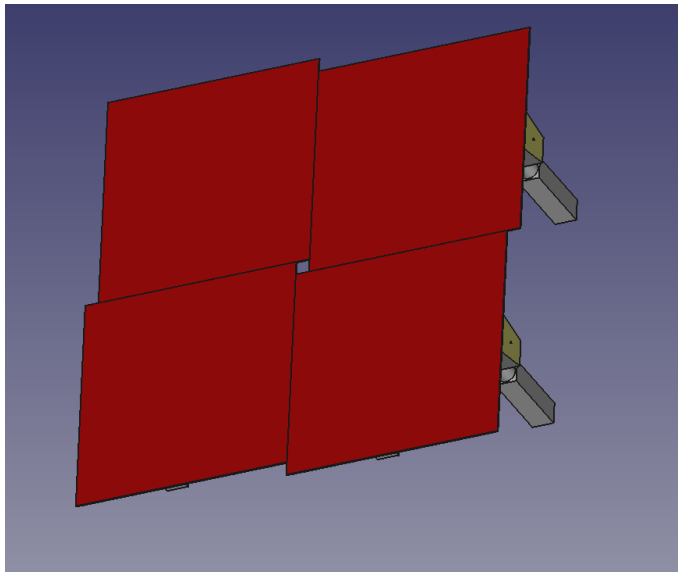
- Module support hosts both mechanical interface and thermal interface connections
- Decoupling of thermal and mechanical interface
- Lean setup with low mass and small heat capacitance
- Effective thermal decoupling from outside world
- High flexibiliy on mechanical interface solutions
- Mechanical interface serves as support for HICs (Hemisphere Interface Cards)



# Mosaic formation

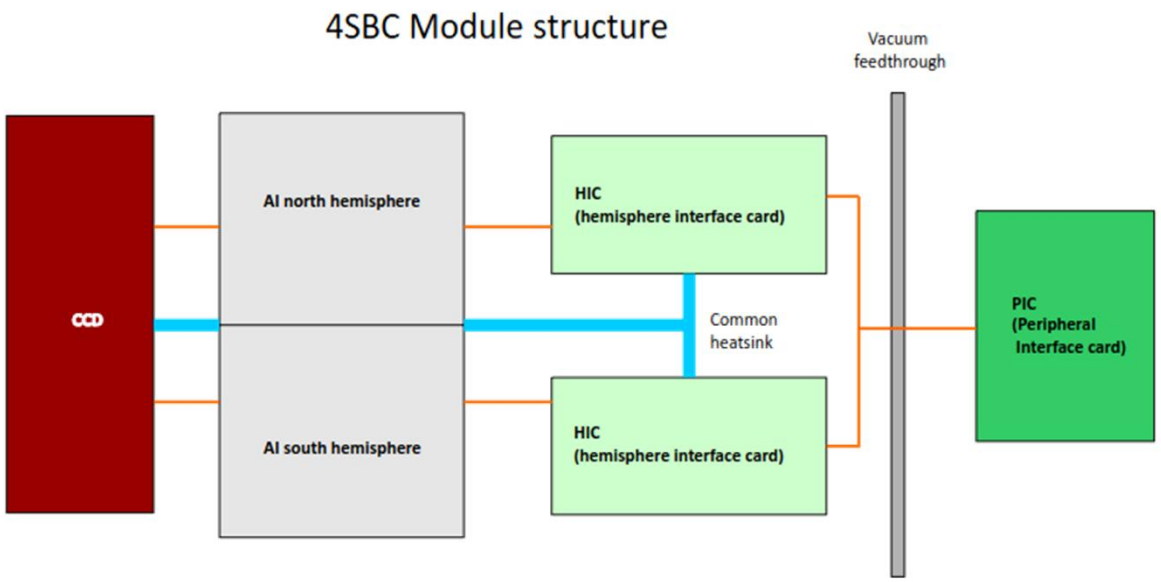
- Unobstructed field of view
- Large areas / arrays of arbitrary size
- Common support structure
- Coolant distribution panel
- Each module w/ own electrical backend / DAQ





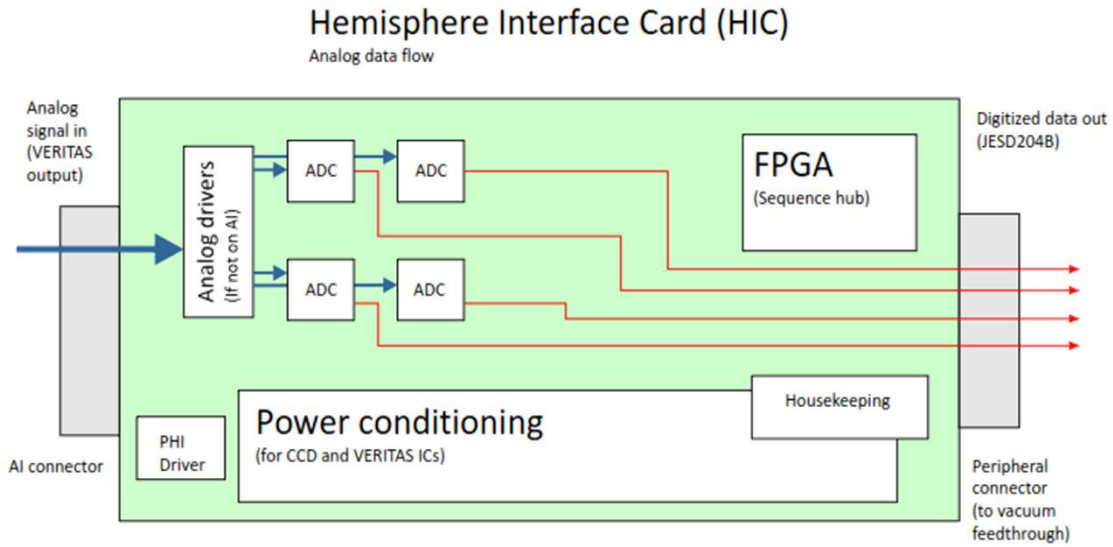
"LAMP-ish" configuration w/ opening for primary beam

# 4SBC Module



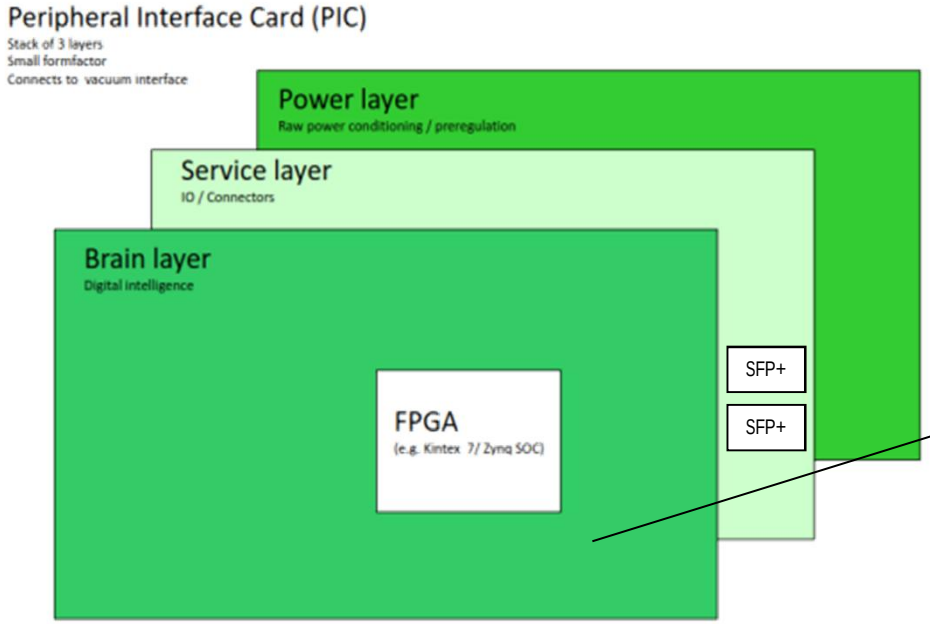

- Stand-alone module configuration
- Cable between PIC and HIC allows for flexible installation scenarios
- Heatsink interface can be located on different flange

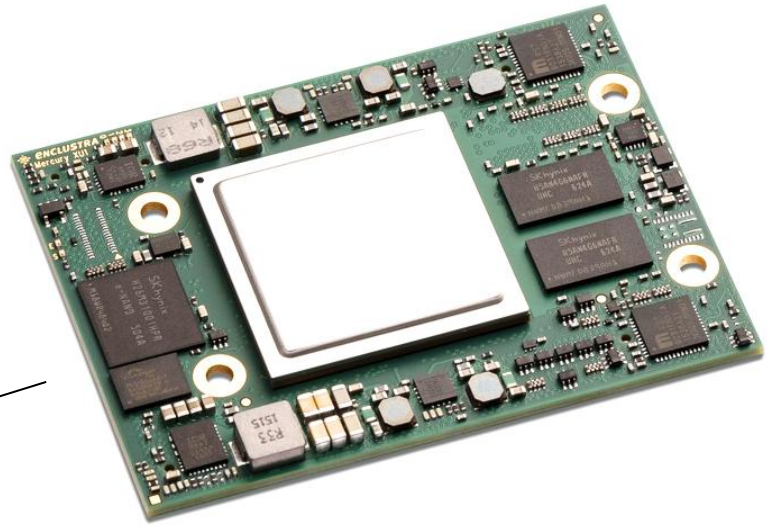
# 4SBC electrical backend




- Digitization of serial analog data output from VERITAS ICs
- Fast JESD compatible multichannel ADCs / few output lanes

# 4SBC electrical backend



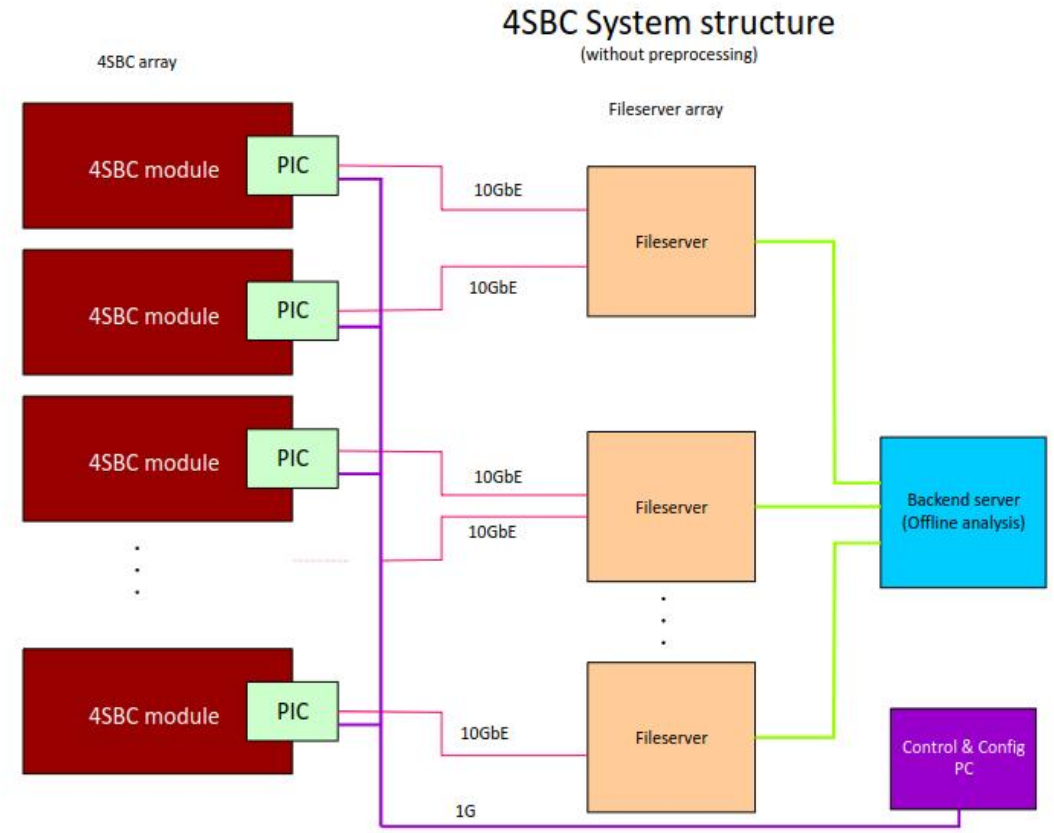
- PIC is interface to outer world and data acquisition system
- "3 layer" approach for maximum flexibility and modularity
  - "Power layer": raw supplies for HIC
  - "Service layer": offers connectivity periphery
  - "Brain layer": FPGA based preprocessor / data wrapper

- Commercially avaliable Mercury XU1+
- Xilinx® Zynq Ultrascale+™ MPSoC
- 4GB DDR4 ECC SDRAM
- 16 × 6/8/12.5 Gbit/sec MGT
- 2 × Gigabit Ethernet
- Up to 747,000 LUT4-eq
- Small form factor (74 × 54 mm)

# 4SBC System structure

Massive parallel readout approach:

- Complete acquisition of entire data
- Constant data rate of 1.7 GByte / s per module
- Brain layer serves mostly as data wrapper
- Maybe minor (reversible) preprocessing tasks
- Sever rack for data storage
- 1 Fileserver for every two modules
- 1 Backend server for processing and offline analysis
- Array of 2 x 2 4SBC tiles yields total volume of 6.8 GByte /s
- "Zero suppression" introduces occupancy-depending data reduction
- "Lossless compression" on Brain layer FPGA possible to save storage space



# Summary & Conclusion

System design:

- weighted mean of manifold requirements
- TrueTile module approach serves as a platform for integration of large area sensors and sensor arrays
- 4SBC system will server as a pathfinder for future TrueTile systems
- System design considers large variety of aspects
  - Application
  - Spatial
  - Data rate
  - Power
  - Thermal