Ultimate throughput and energy resolution of analog pulse processing front-ends

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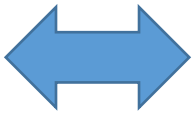
High-throughput and high-resolution EDS systems

Motivation: evolution of X-ray detection systems to provide the high-rate performances further challenged by ongoing synchrotron upgrades or future sources (a factor 10-100 to beam-on-sample fluxes increase expected)

high count rate capability (>1Mcounts/s/ch)
- small processing time
- pile-up management and minimum dead time (max. OCR vs. ICR)

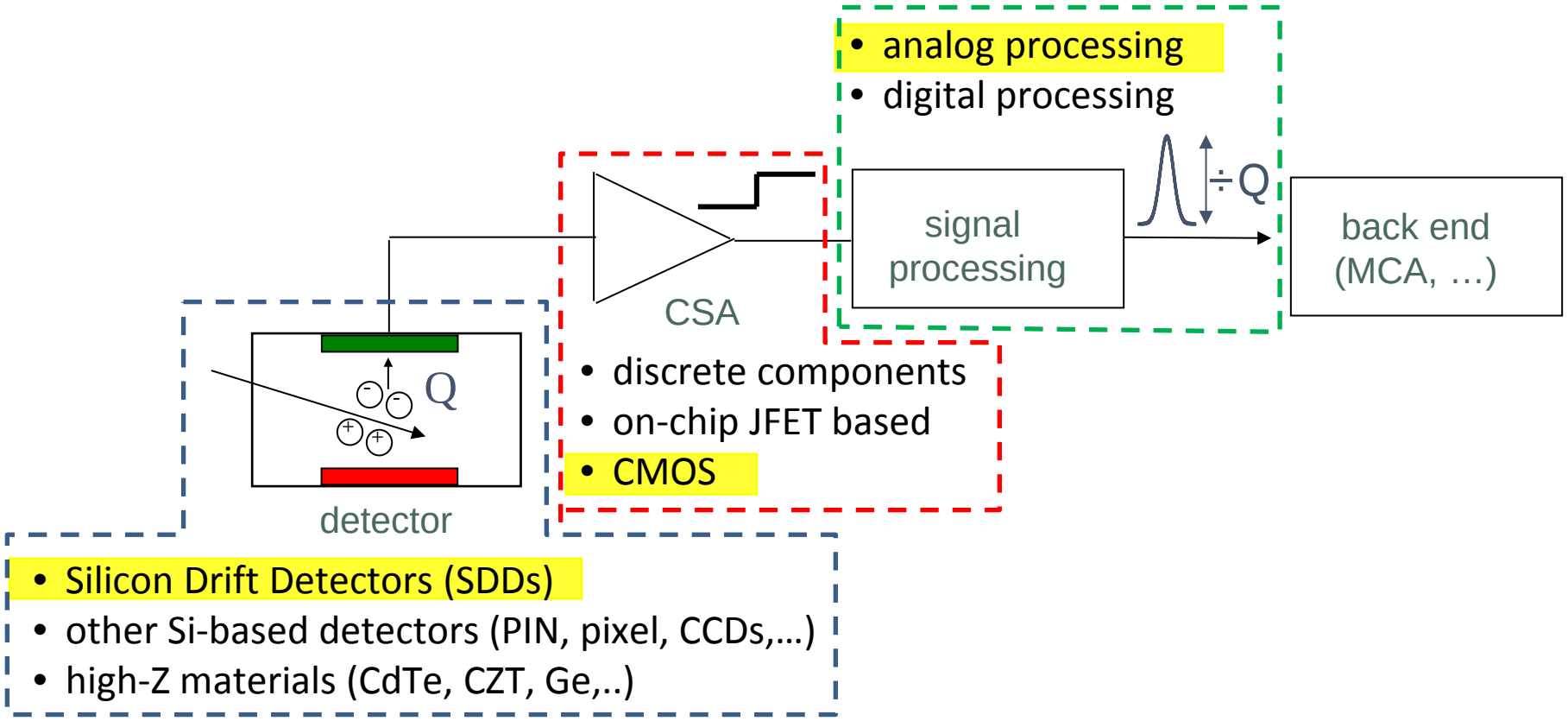


good energy resolution
- optimum energy resolution close to Fano limit (~122eV @6keV in Silicon)
- good low-energy response

trade-off strategies:
- processing time
- processing type (analog/digital)

This talk will focus on the limits assessable with analog integrated electronics (preamplifier+analog signal processing).
The talk will not be a review but a (personal) overview of the main parameters to be optimized and their limits.

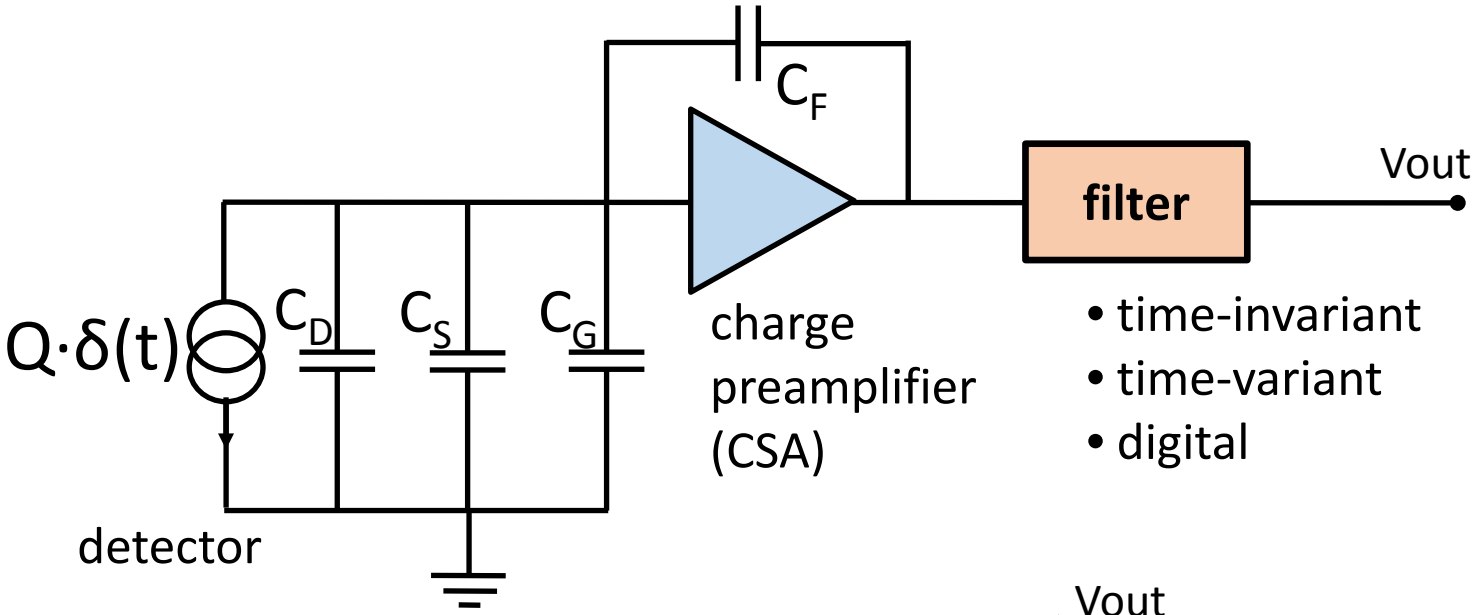
The electronics FE and processing chain for EDS detectors



Main limitations in the high-throughput and high-resolution trade-off

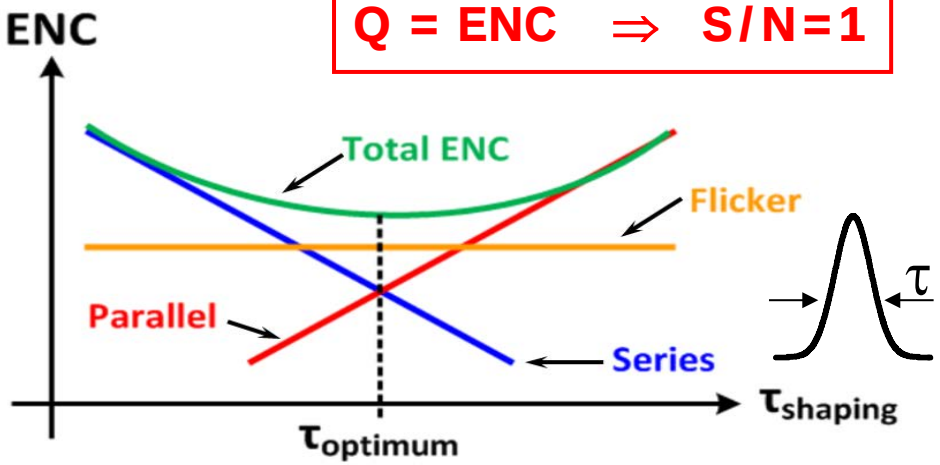
- Electronics noise
- Ballistic deficit
- Pile-up
- Count-rate capability (max OCR, OCR vs. ICR)

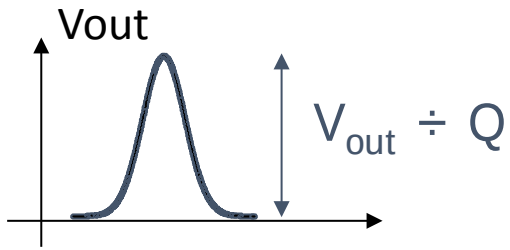
Electronics noise

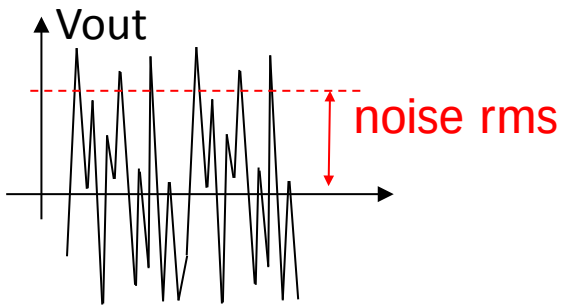


- time-invariant
- time-variant
- digital

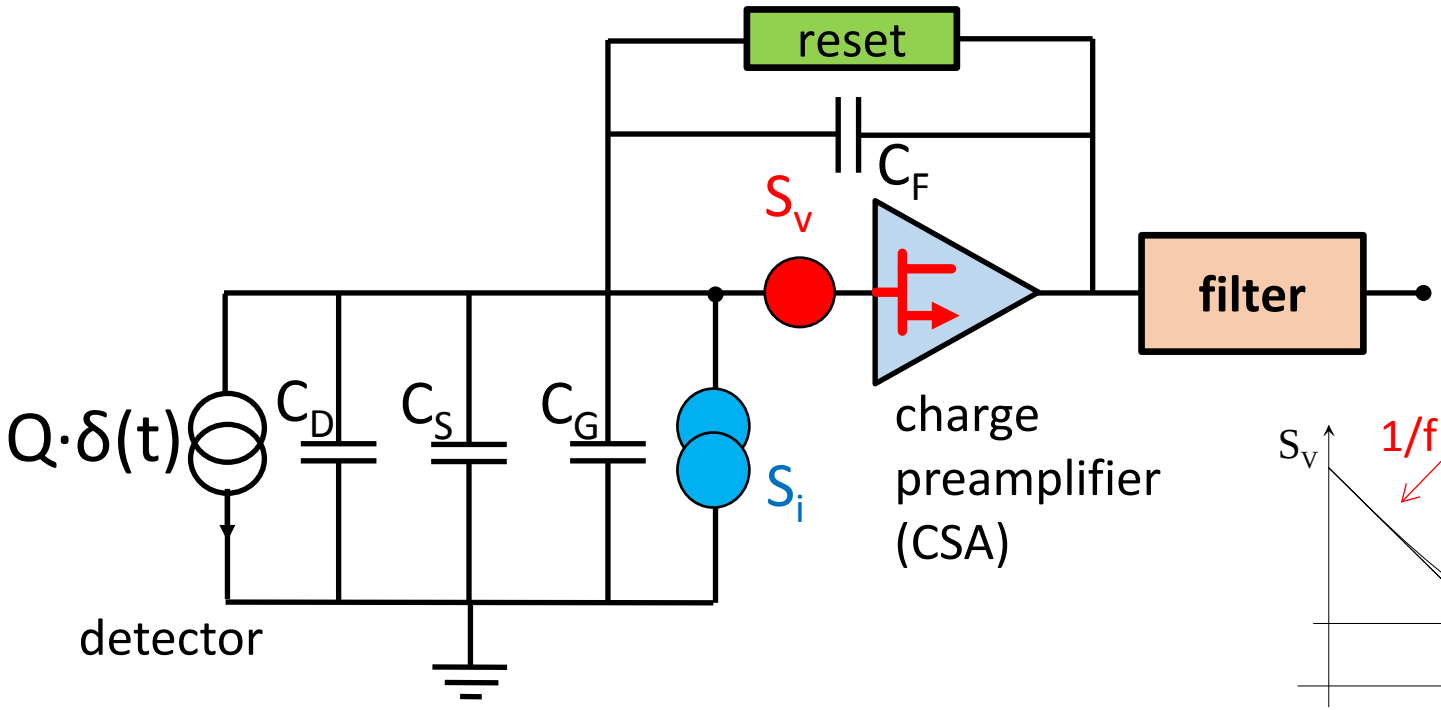
Q = ENC ⇒ S/N=1



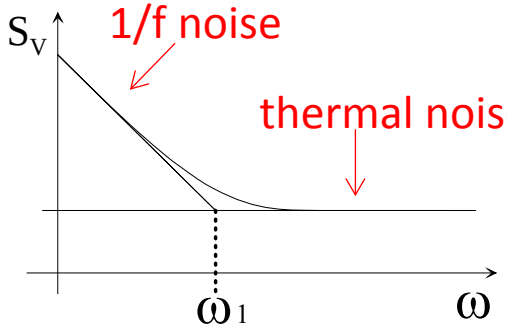




Electronics noise contributions



input FET noise contributions:

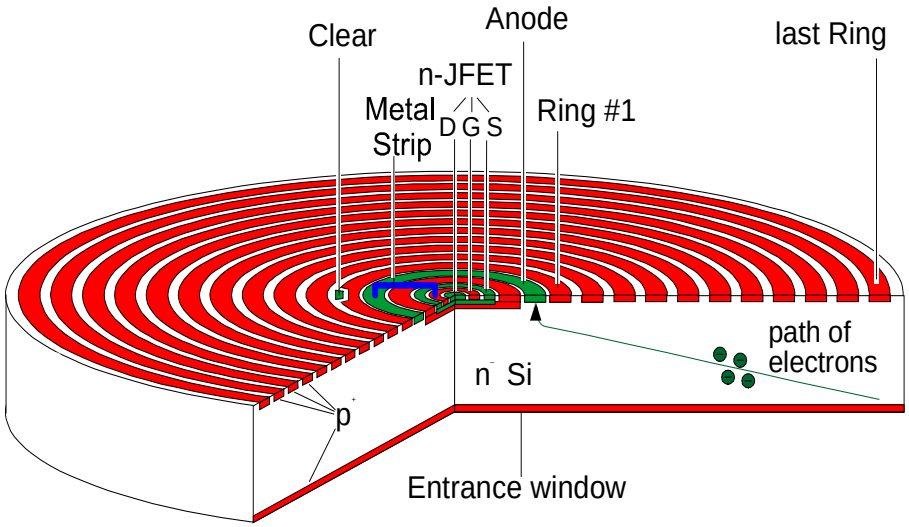


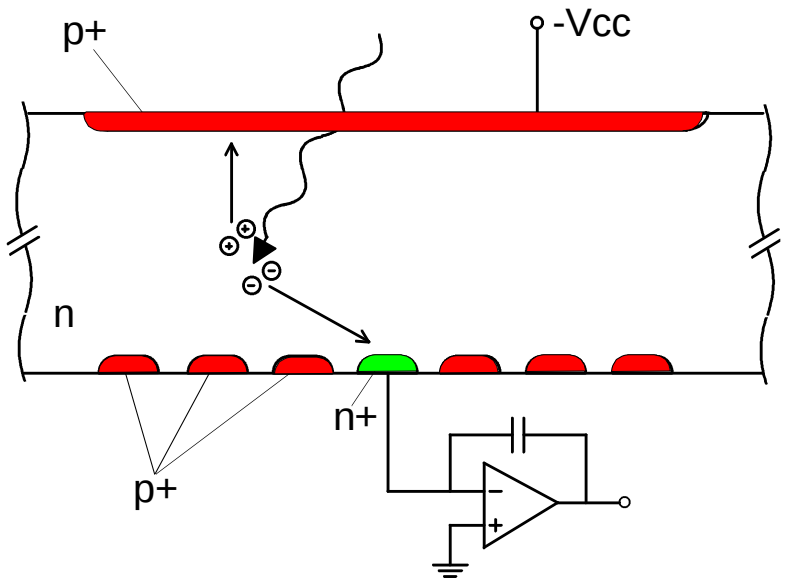
$$ENC^2 = A_1 4KT\alpha \frac{C_T^2}{gm}\frac{1}{\tau} + A_2 2\pi A_f C_T^2 + A_3 2qI_{leak}\tau$$

series 1/f parallel

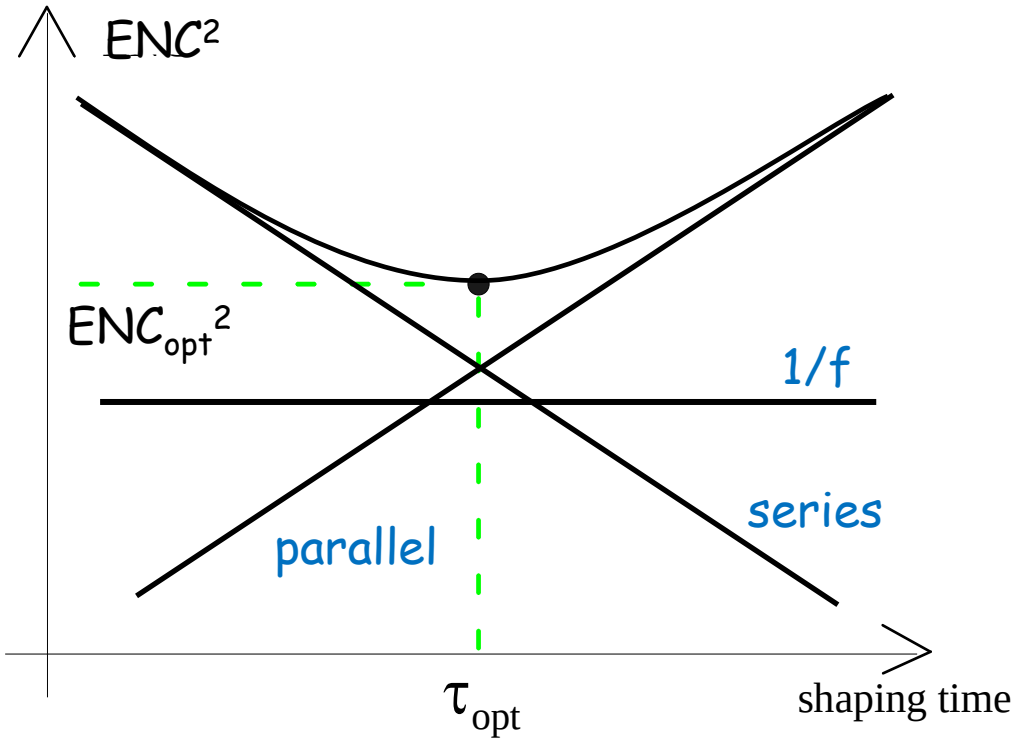
$C_T = C_D + C_S + C_G + C_F$
C_D : detector cap.
C_S : parasitic cap. (bonding, pads,...)
C_G : gate cap. of input FET
C_F : feedback cap.
gm : transconductance of input FET
A_f : 1/f noise coeff. of input FET

Front-end for Silicon Drift Detectors





- JFET integrated on the SDD
  - lowest total anode capacitance
  - easier interconnection in SDD arrays
  - limited JFET performances (gm, 1/f)
  - sophisticated SDD+JFET technology
- external FET (JFET, MOSFET)
  - better FET performances
  - standard SDD technology
  - larger total anode capacitance
  - interconnection issues in SDD arrays



Electronics noise with ext. MOSFET

- alternative solution to improve series noise contribution, which dominates in high-rate operations
- C_T^2/gm factor benefits of large gm of MOSFET, despite increase of C_T due to external connection
- 1/f noise contribution (A_f) should be minimized for optimum resolution

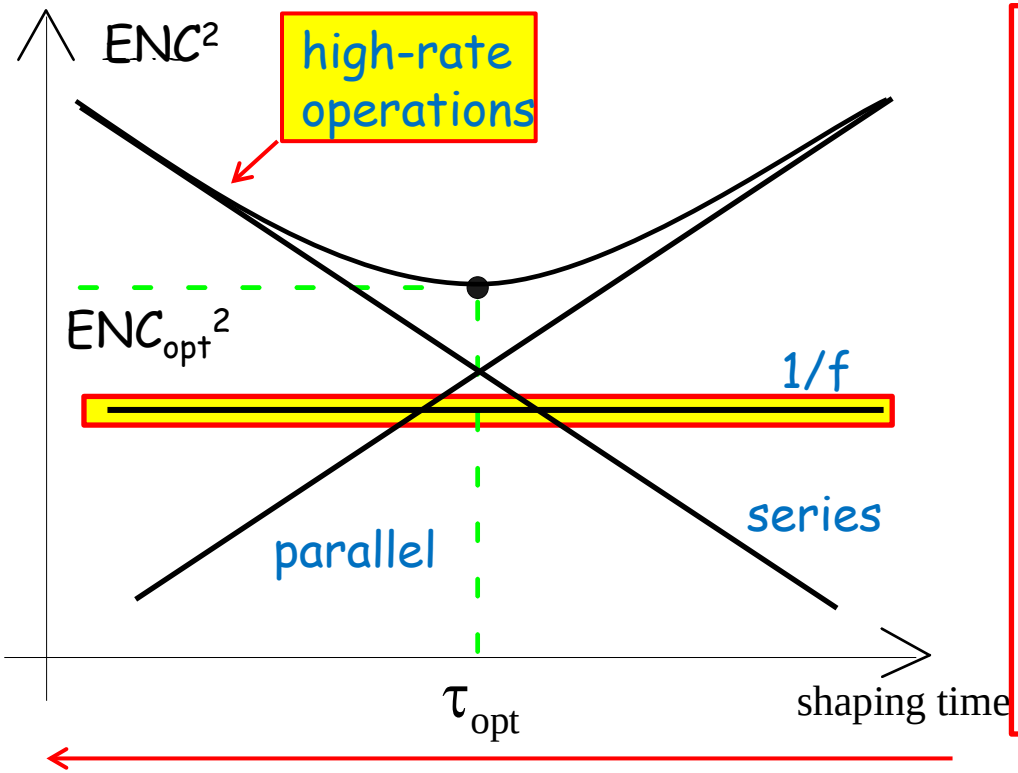
$$ENC^2 = A_1 4KT\alpha \frac{C_T^2}{gm}\frac{1}{\tau} + A_2 2\pi A_f C_T^2 + A_3 2qI_{leak}\tau$$

series 1/f parallel

PMOSFET preamplifiers:

- …
- G.Bertuccio, S.Caccia, NIMA 579, p. 243, 2007.
- G.De Geronimo, et al., IEEE TNS, vol.57,3, p.1653, 2010.
- L.Bombelli, et al., IEEE NSS Conf. Rec., 2010.

Electronics noise minimization (for high rates operations)



series white noise:

$$gm\,(I_D) \div \frac{I_D}{nV_T} \div I_D \quad \text{(weak inversion: } V_{GS} \ll V_{th})$$

$$ENC_S^2 \div \frac{(C_D + C_S + C_G)^2}{I_D}$$

- minimize C_S
- minimize C_G (but → mod. inv. $V_{GS} \sim V_{th}$)
- (rather indep. from L_{min}, but W,L small for C_G)
- increase I_D (vs. power, biasing limitations, …)

1/f noise:

$$ENC_{1/f}^2 \div A_f(C_D + C_S + C_G)^2$$

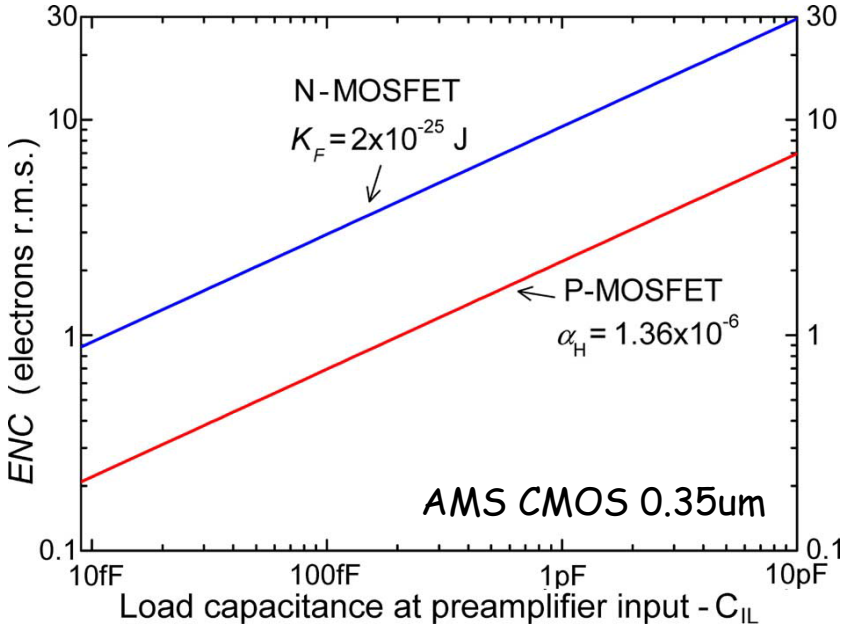
- minimize C_S
- A_f depends on nMOS/pMOS, W,L (C_G), I_D, technology….

$$ENC^2 = A_1 4KT\alpha \frac{C_T^2}{gm}\frac{1}{\tau} + A_2 2\pi A_f C_T^2 + A_3 2q\cancel{I_{leak}}\tau$$

(cooling, short τ_{sh})

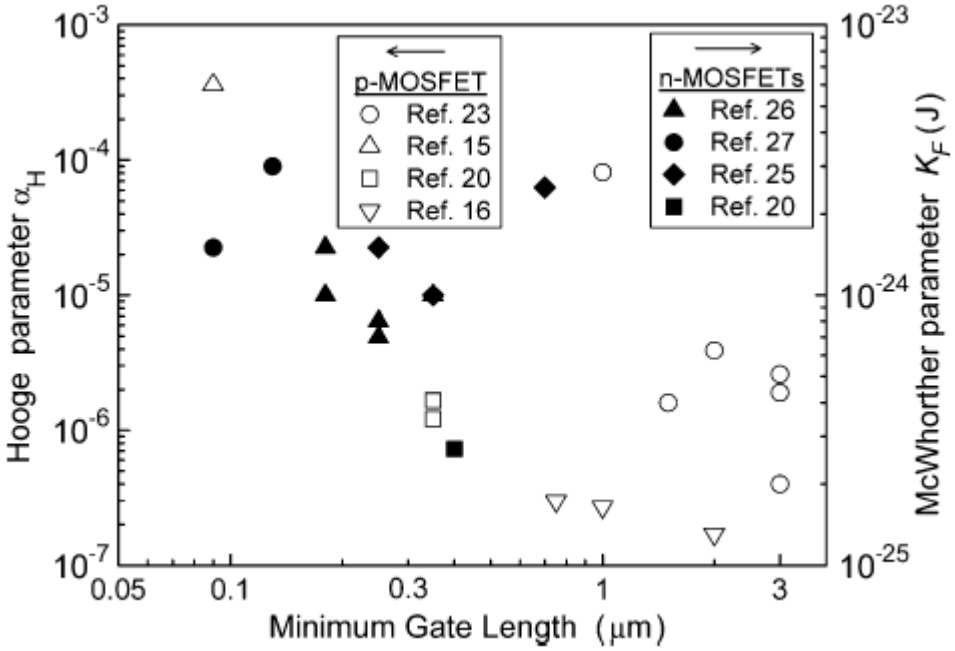
series 1/f

PMOS vs. NMOS



(G.Bertuccio, S.Caccia, TNS, 2009)

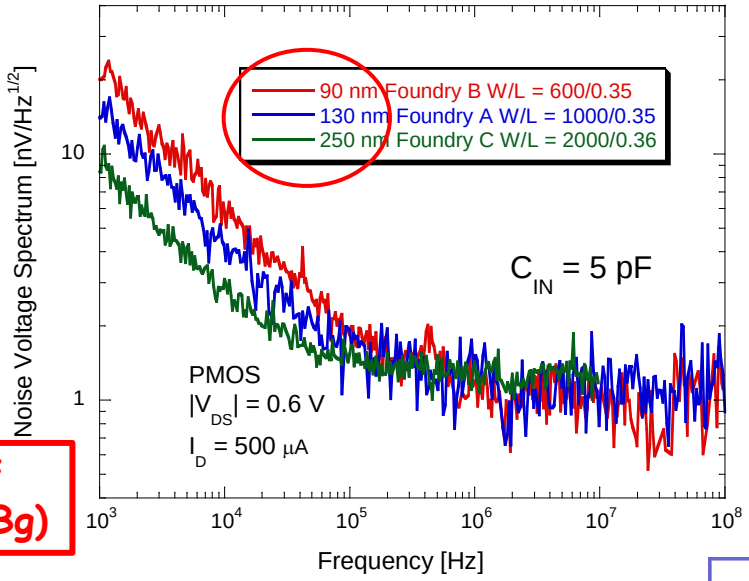
1/f noise vs. technologies



1/f noise vs. scaling

- less difference between NMOS and PMOS
- PMOS: 1/f appears to increase with scaling

(many measurements and papers on noise vs scaling...)

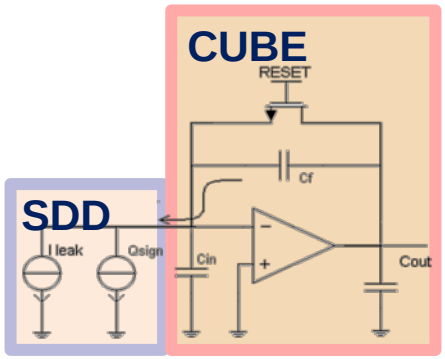


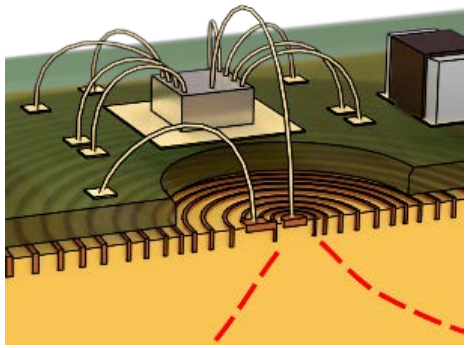
courtesy of V.Re (Uni-Bg)

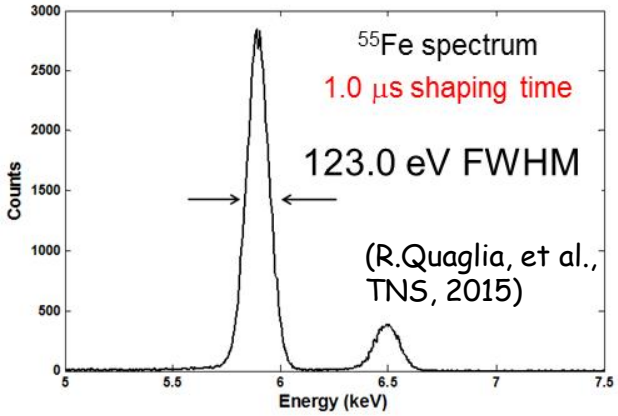
CMOS Preamplifier 'CUBE' (L. Bombelli, et al., NSS Conf. Rec., 2011)

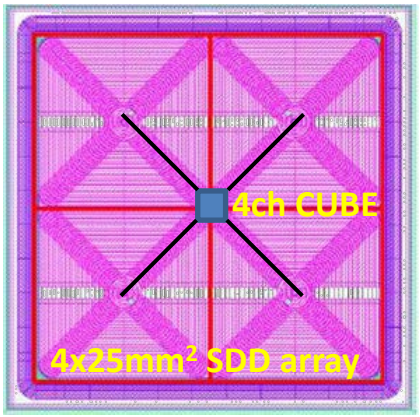
- **the whole preamplifier** is connected close to the SDD (and not only the FET):
- the remaining part of the electronics (the **ASIC of analog processing or a DPP**) can be placed relatively far from the detector (even 10-100 cm)
- **the high transconductance** of the input MOS compensates the larger capacitance introduced in the connection SDD-FET

$$ENC^2 \div \frac{C_T^2}{gm}\frac{1}{\tau}$$

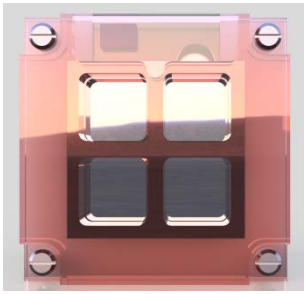


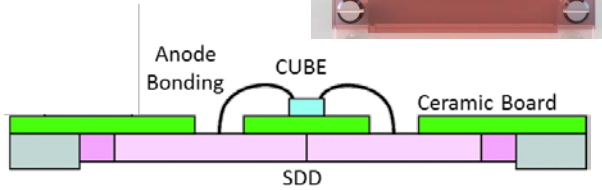


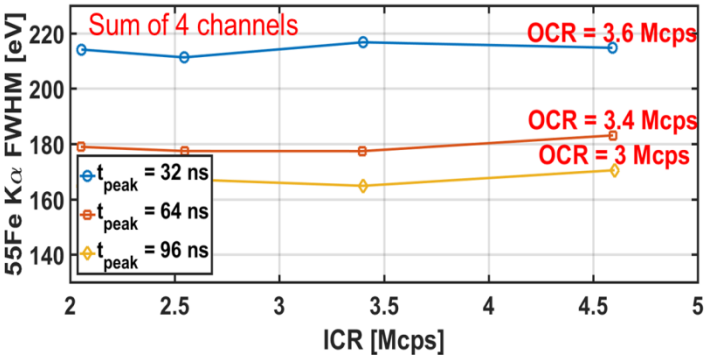




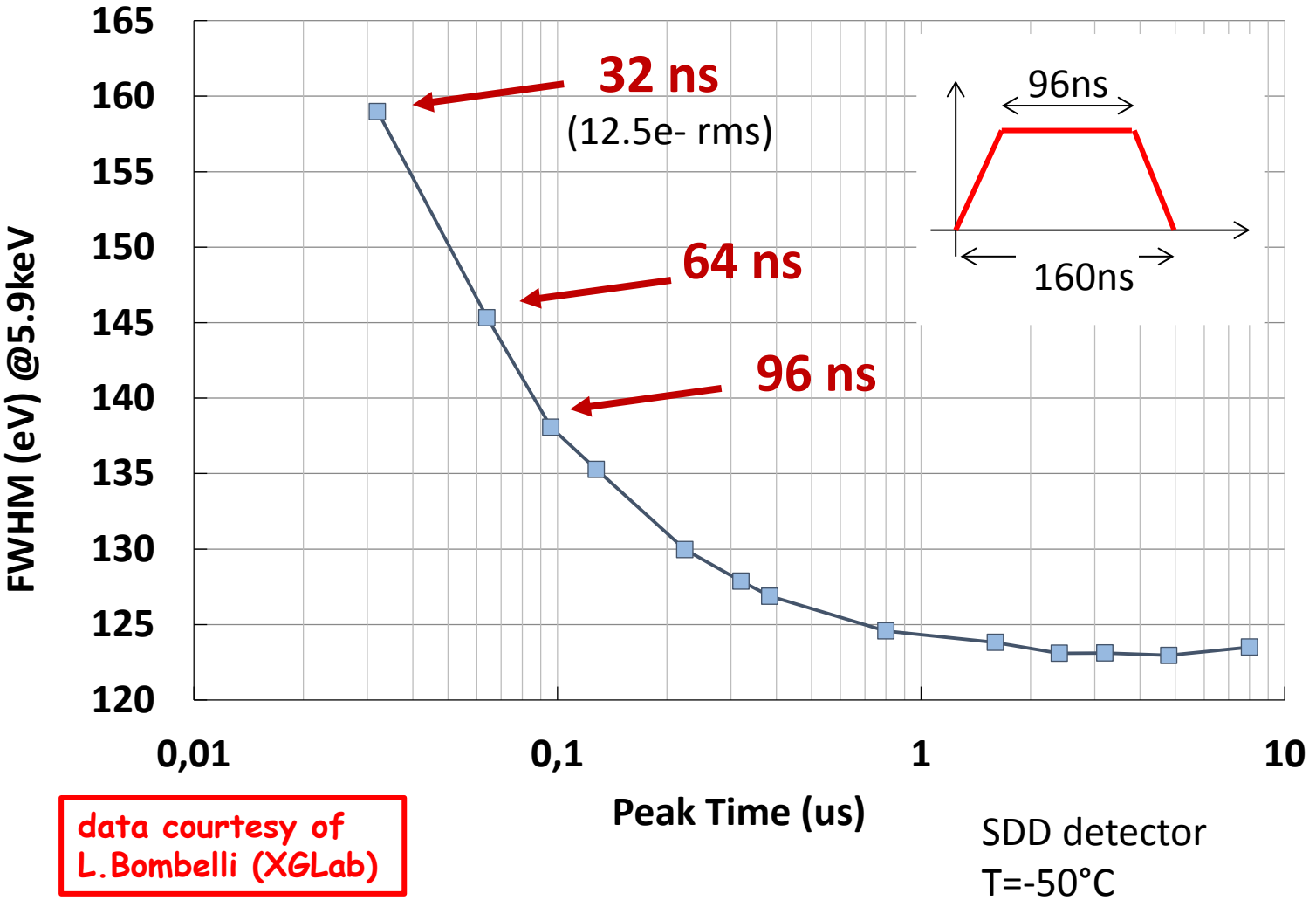
Monolithic 4 channels CUBE preamplifier for ARDESIA module







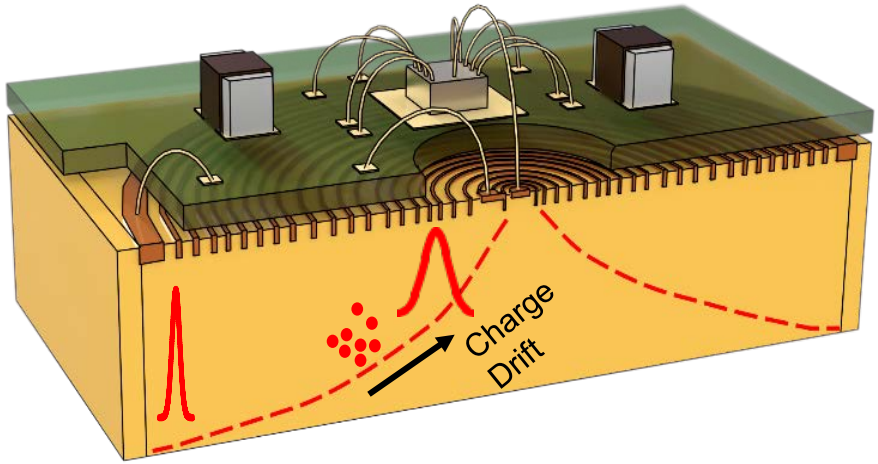
Energy resolution with CUBE

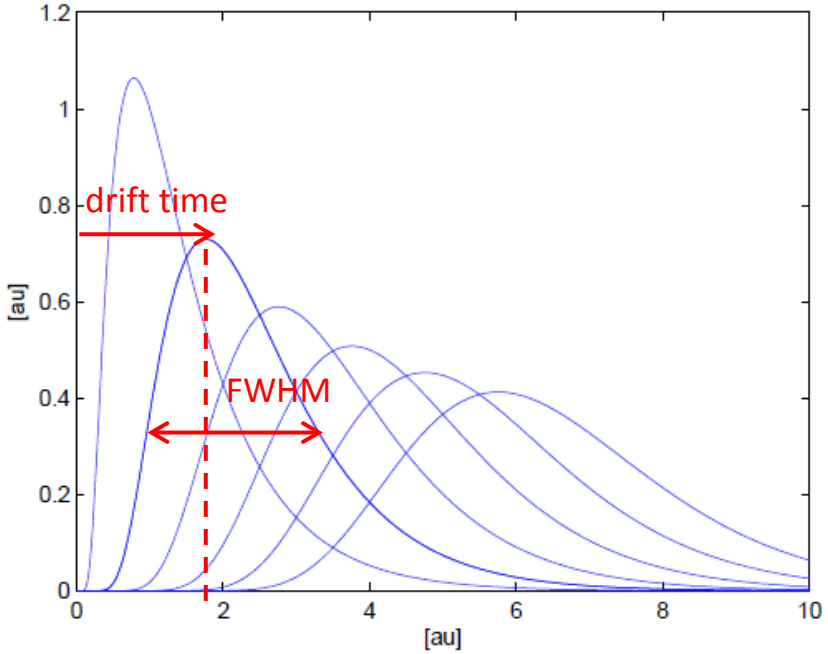


data courtesy of L.Bombelli (XGLab)

SDD detector
T=-50°C
DANTE DPP (XGLab)

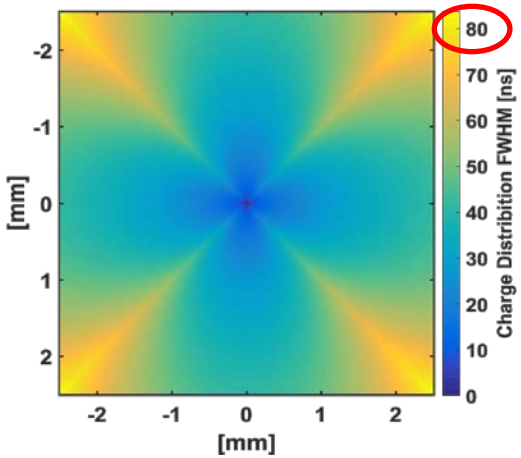
Ballistic deficit (1)



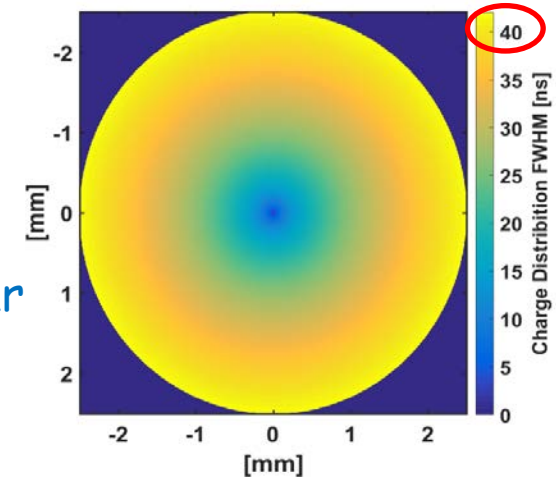


- Diffusion of the charge packet while drifting towards the anode
- The width of the current pulse at the anode depends on the generation point

square SDD

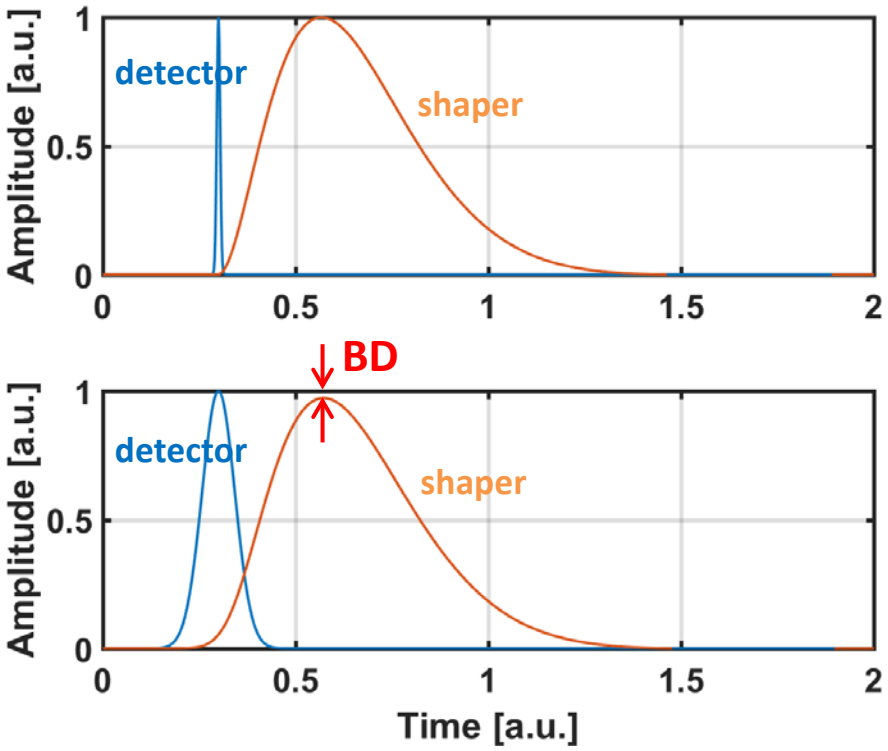


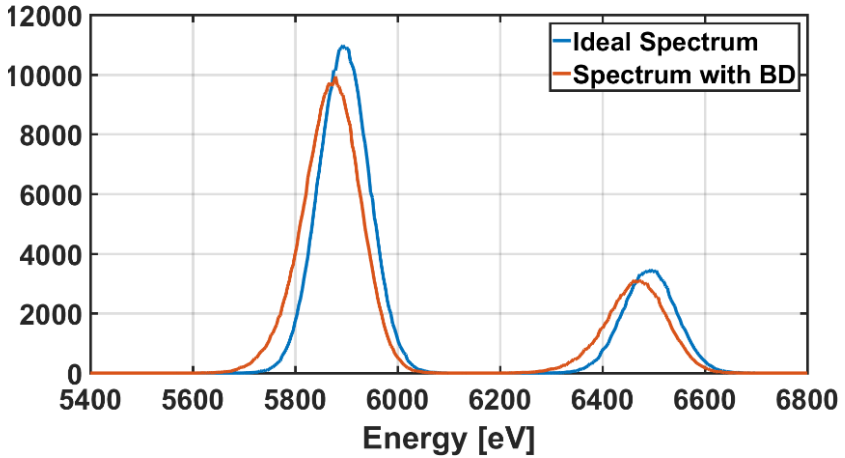
circular SDD



(data from simulations)

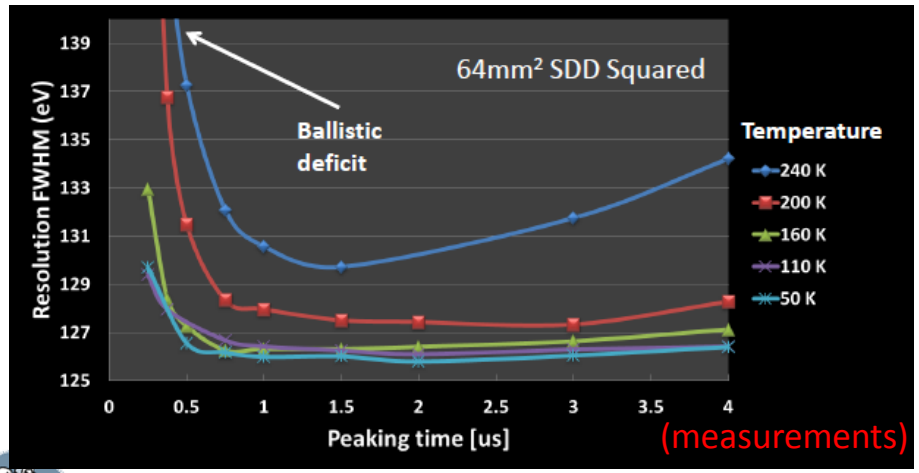
Ballistic deficit (2)

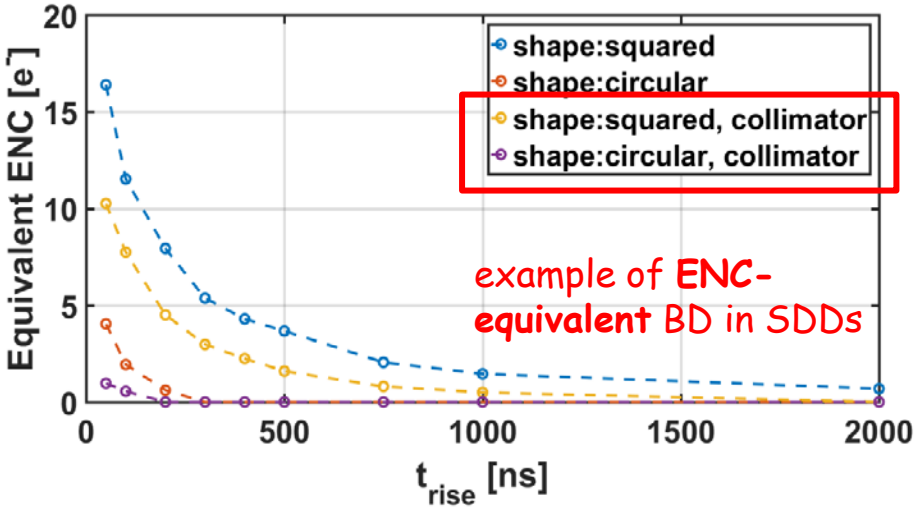




With detector pulse width comparable to the shaping time, the filter peak output decreases

The energy spectrum broadens and the peaks move towards lower energies





→ be aware for minimum pulse duration

CSA discussion: performances

- Improvement of CMOS CSAs noise at short processing time still possible (although maybe not terrific..)
- still room for minimization of parasitic capacitances (bonding, pads, stray…). Bump-bonded SDD arrays+ASIC an option to be explored? Other specific interconnection development?
- Further shortening shaping time @ constant noise:

$$\frac{C_T^2}{gm}\frac{1}{\tau} = \frac{ENC^2}{const} \quad \Rightarrow \quad \tau \div C_T^2$$

$$\tau \div 1/gm \quad \text{(but remember gm and } C_G \text{ dependency)}$$

Questions to be addressed:

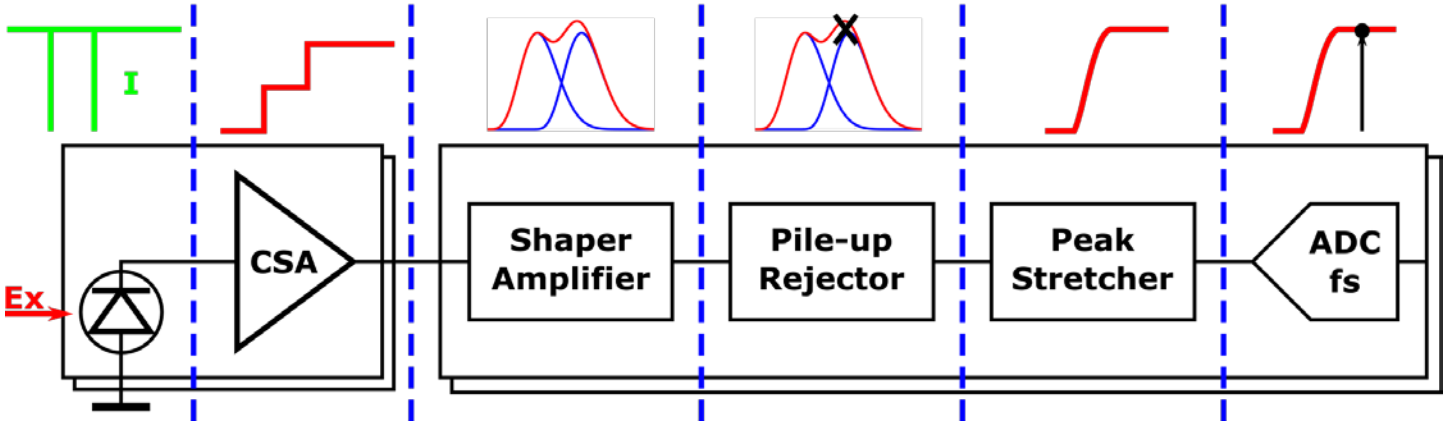
- further reduction of C_T?
- further increase of gm?
- then overall processing time reduction limited by ballistic deficit?

  → detector segmentation with smaller pixels?

CSA discussion: design methods

- Several models (including simulator ones) exist to attempt optimization of MOSFET design and operation point. Differences in technologies play a role to minimize series and 1/f noise.
- Despite availability of design rules and models, design of an ultra low-noise CSA for a specific X-ray spectroscopy detector remains a multi-parameter, recursive exercise of 'tailoring' a circuit to 'fit' at the best a detector:

Analog Pulse Processing ASICs for High Count Rate X-ray spectroscopy applications



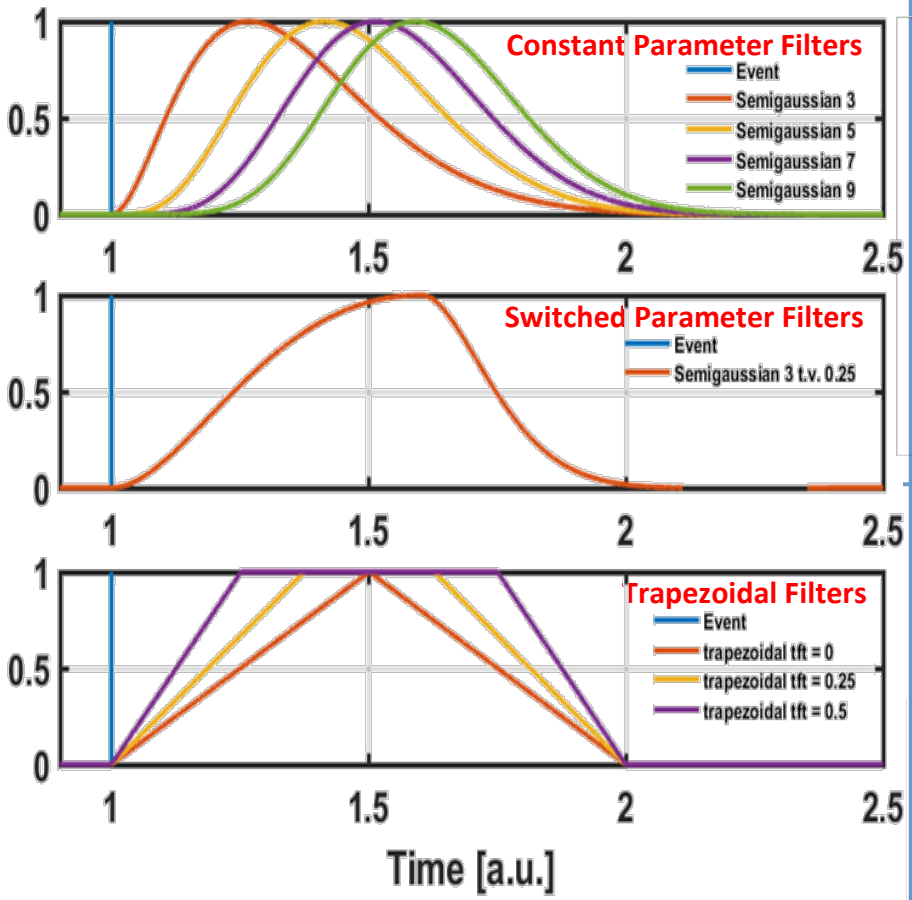
PROS:

- Suitable for large number of channels
- Lower cost per channel
- Lower power consumption
- Suitable for high-integrated detection systems

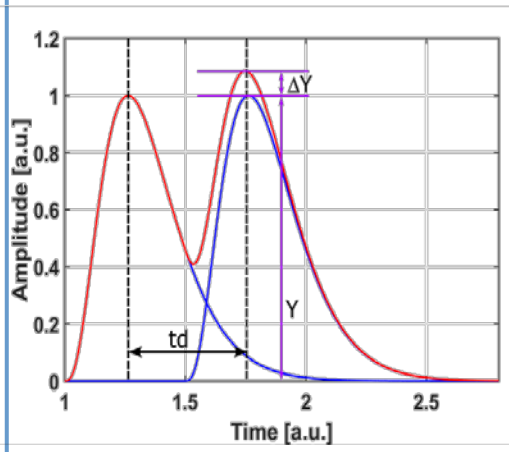
CONS:

- Lower throughput (vs. digital pulse processors)
- Less flexible in filter implementation (shape/duration) and configurability
- Possible higher sensitivity to ballistic deficit at very short processing times

Filter comparisons for high-count rate operations (1)



filters are compared (for the same width @1% of peak amplitude) with respect to three figures of merit:



(1) Pile-up

α_{min} : **minimum distance** so that the amplitude of the second pulse is 1% higher of its real value, normalized to the filter pulse-width.

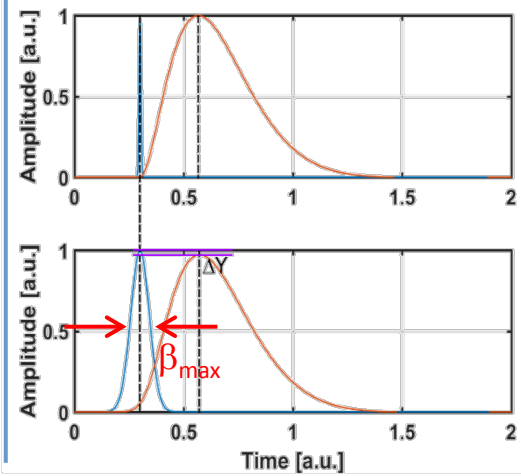
$$FoM_1 = {}^{1}/_{\alpha_{min}}$$

$$ENC^2_{series} = \frac{4kT\gamma}{g_m} C_p^2 \frac{1}{\tau} A_1$$

(2) Noise

series noise coefficient

$$FoM_2 = {}^{1}/_{A_1}$$

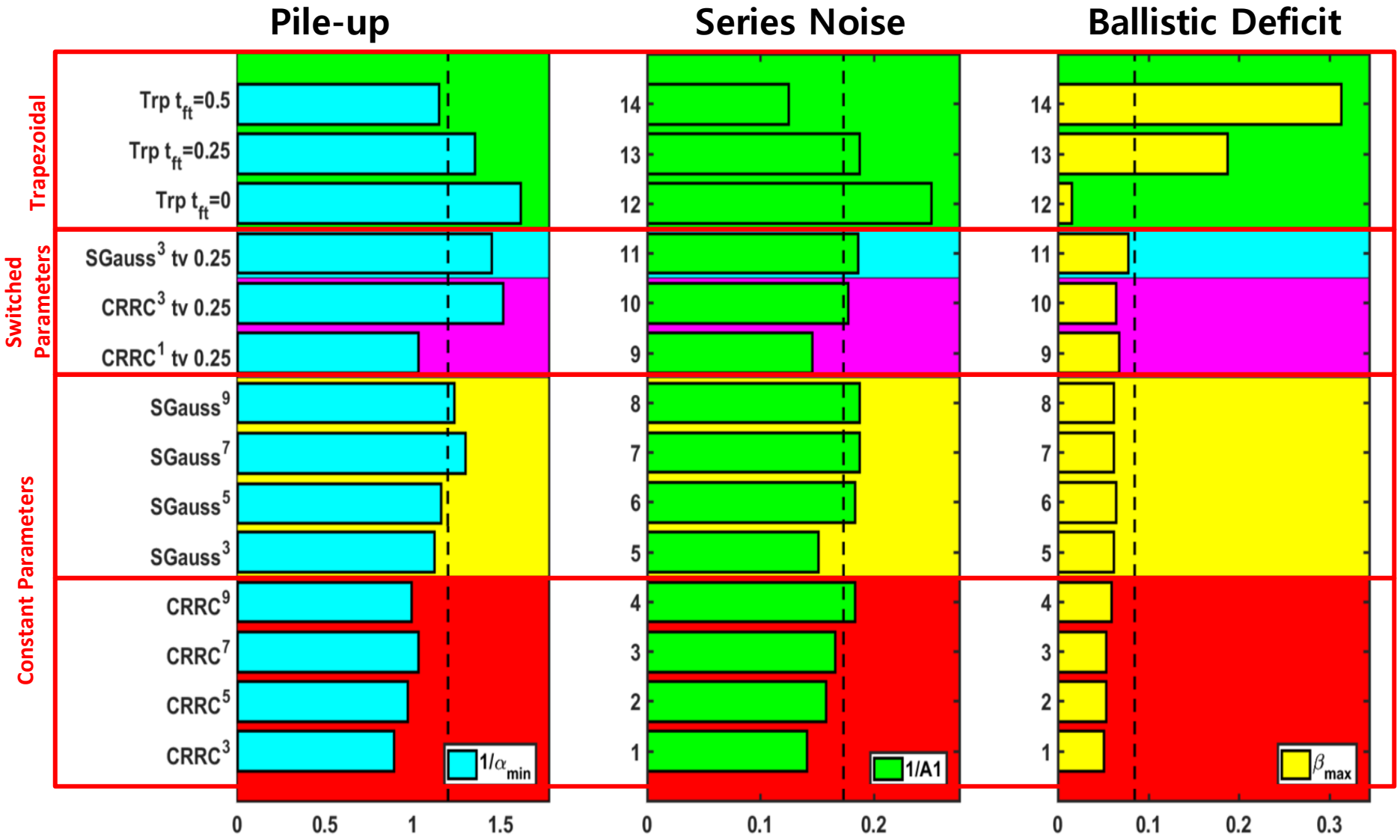


(3) Ballistic Deficit

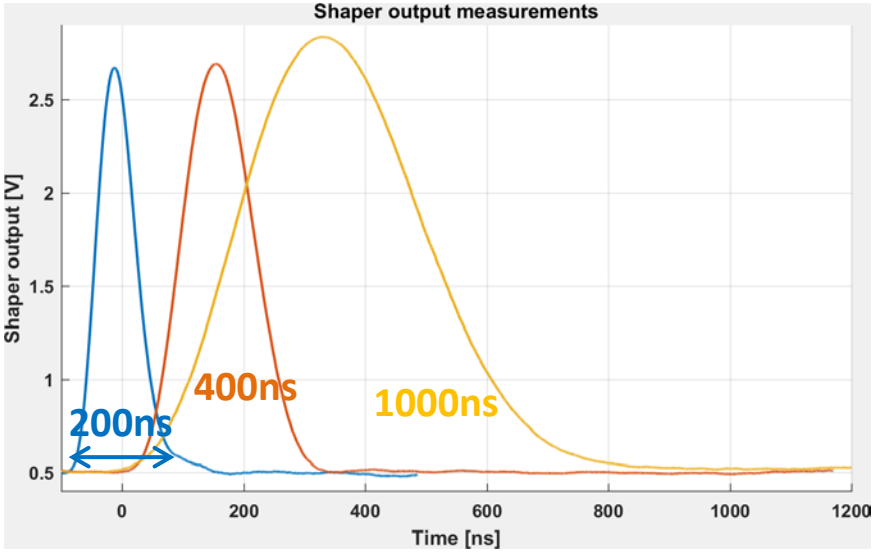
β_{max} : **maximum width** of the input pulse so that the output is 1% smaller than its real value, normalized to the filter pulse-width.

$$FoM_3 = \beta_{max}$$

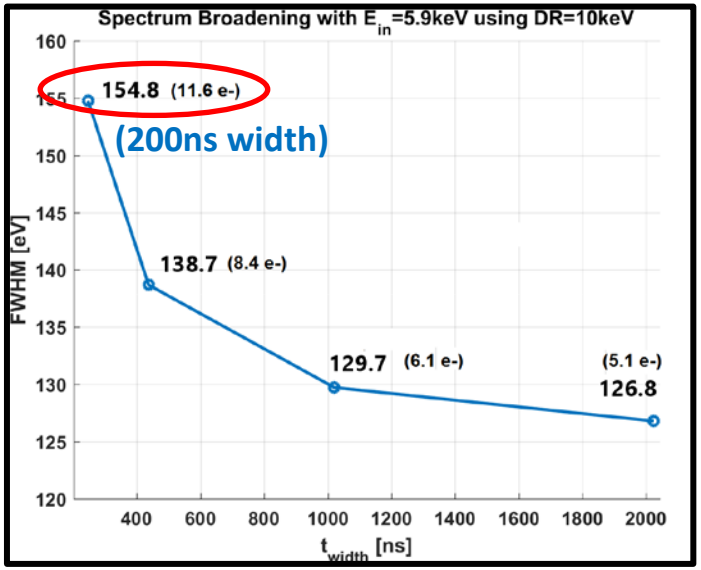
Filter comparisons for high-count rate operations (2)



Shaper pulse shortening (vs. chosen technology)



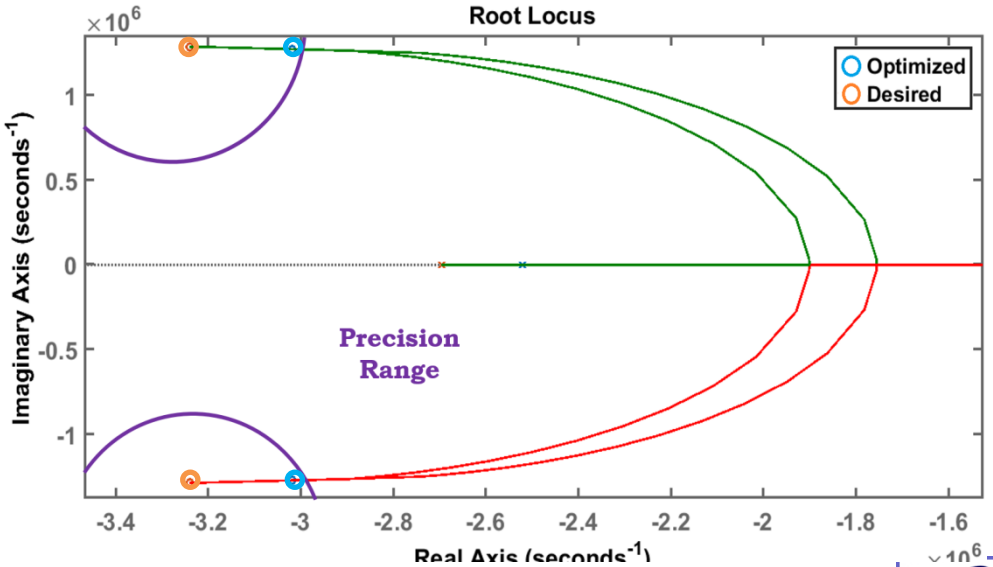
(measurements from TERA ASIC)



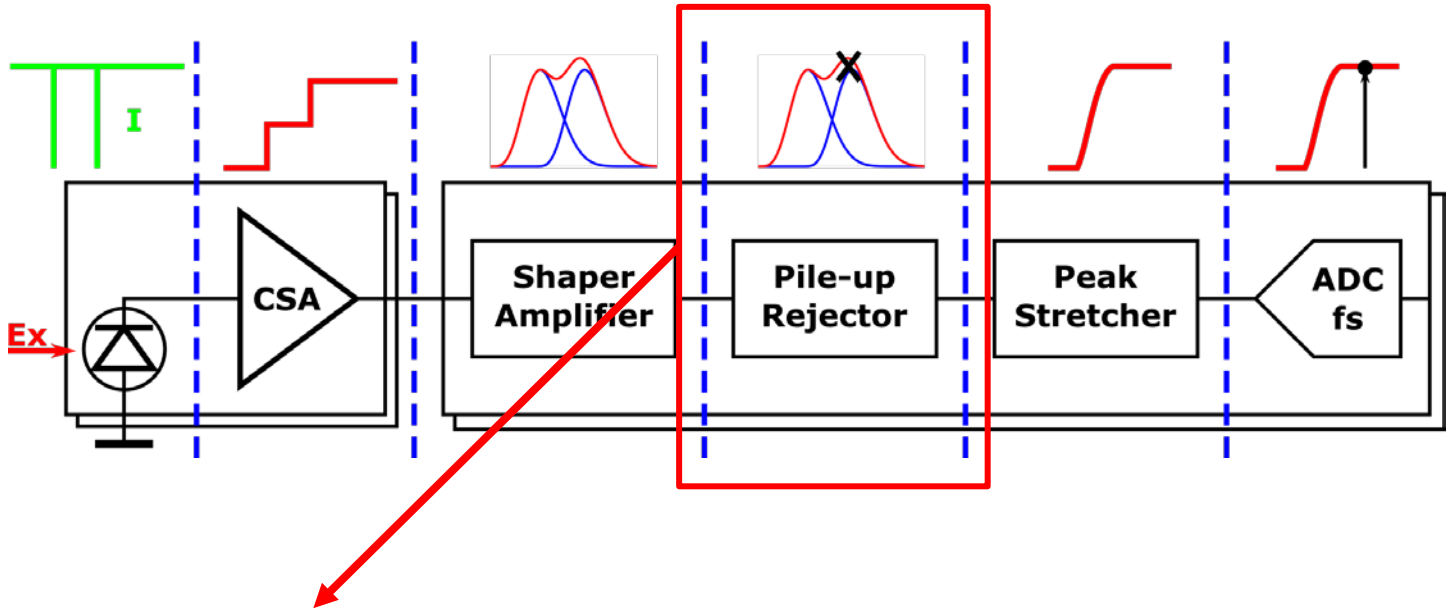
(simulations)

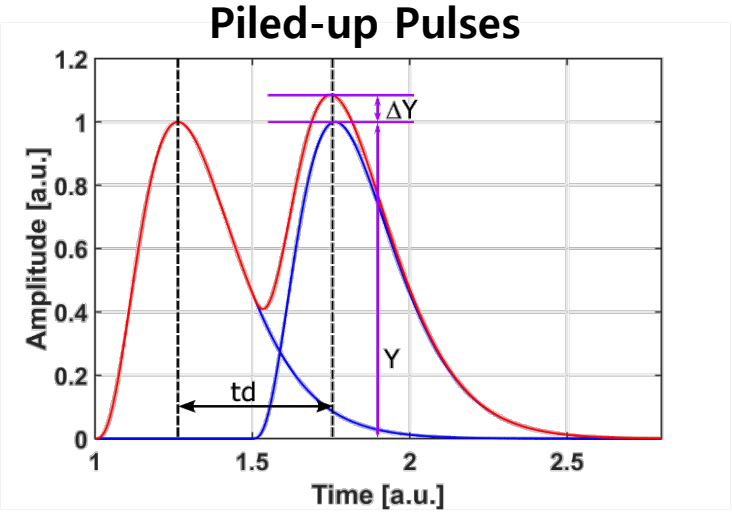
Optimization of electronics noise vs. pulse duration:

- SDD+CUBE
- 0.35μm CMOS technology
- poles tuning vs. bandwidth limitations of the chosen technology



Pile up rejector (PUR)

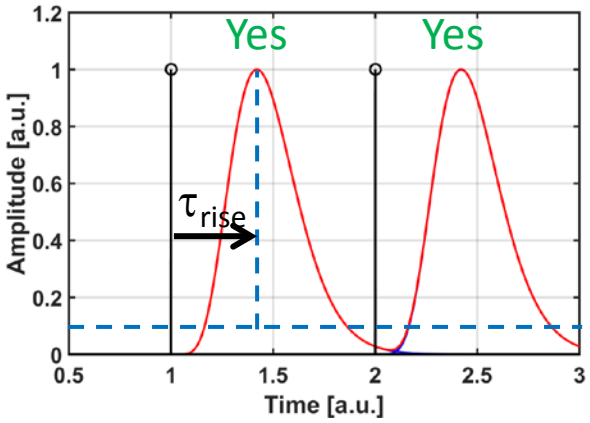


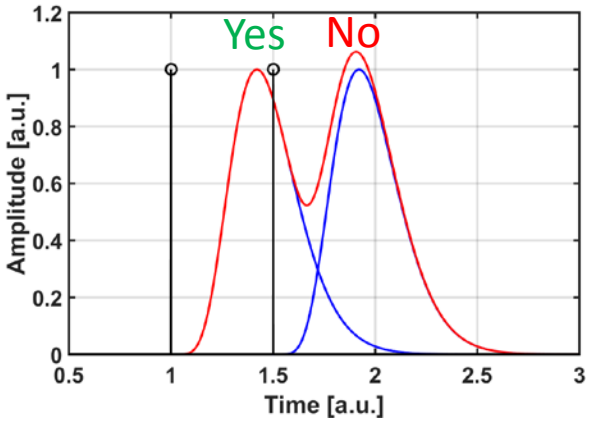


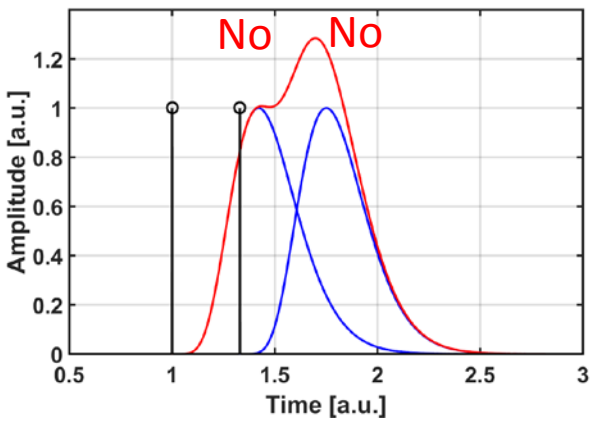
- Pile-up Rejection Algorithm to remove corrupted pulses
- Impact on Output Count Rate limitation

Output Count Rate Limitation: comparison of 2 PUR Strategies

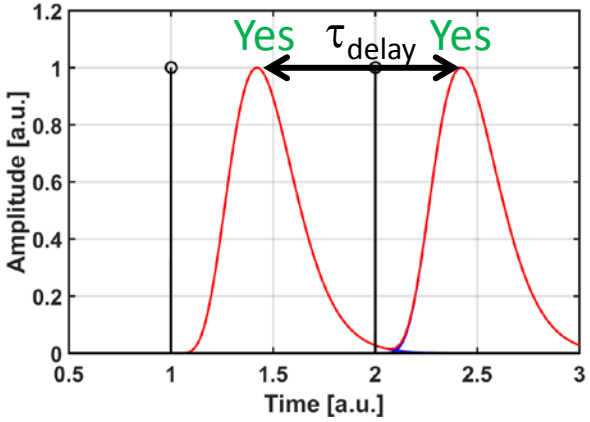
(1) t_{rise} and Low-Threshold based algorithm (De Geronimo, TNS, 2010)



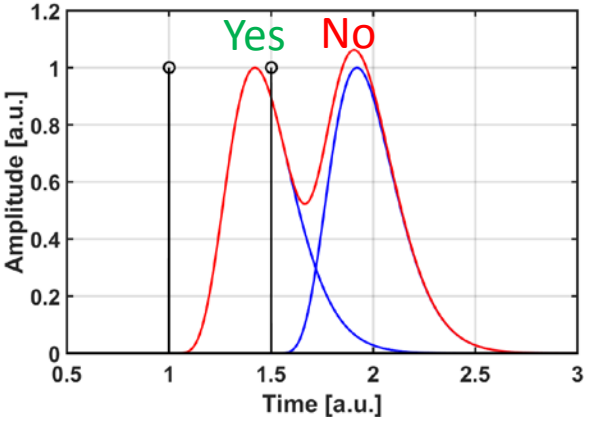




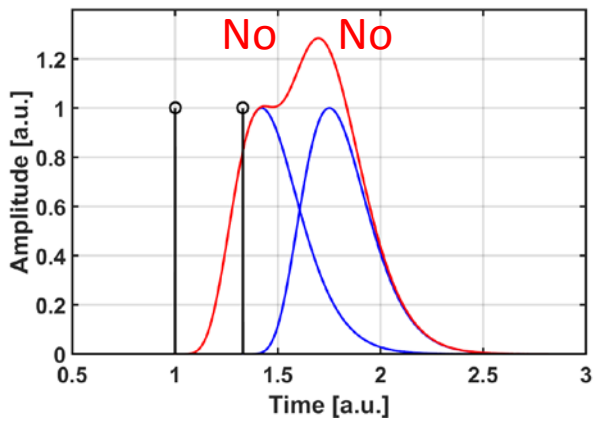
(2) t_{delay} based algorithm (Bellotti, NSS, 2017)



Both pulses acceptable

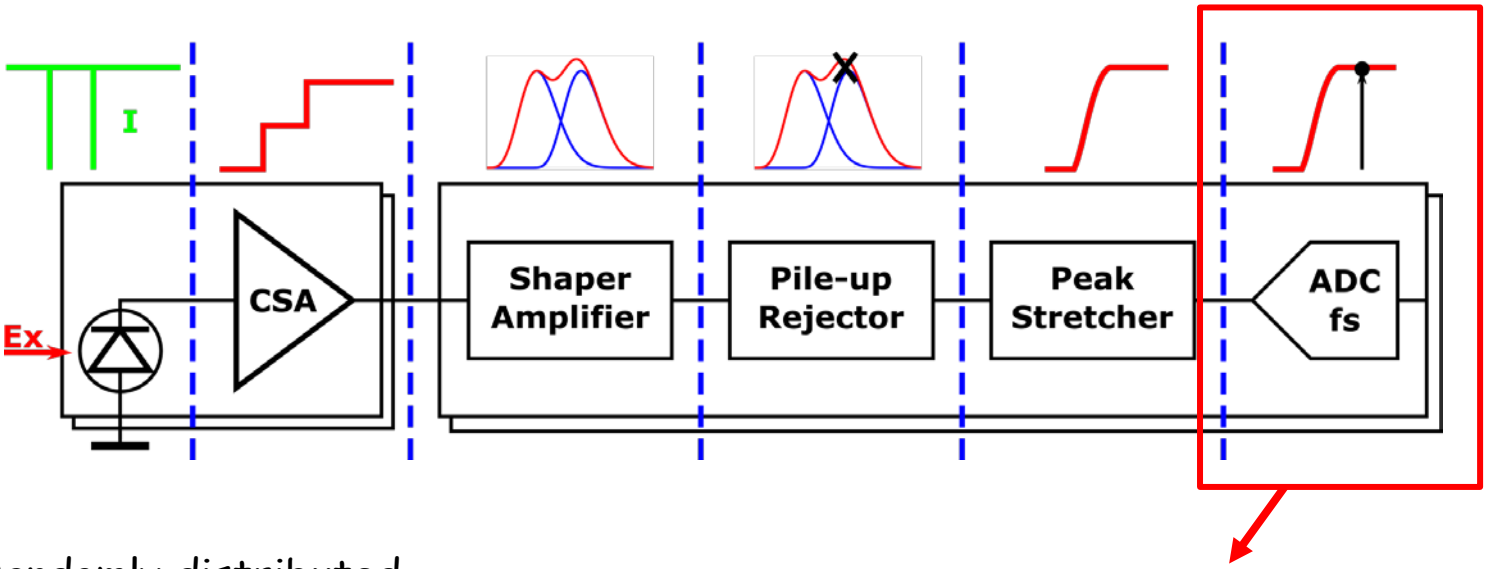


First pulse acceptable



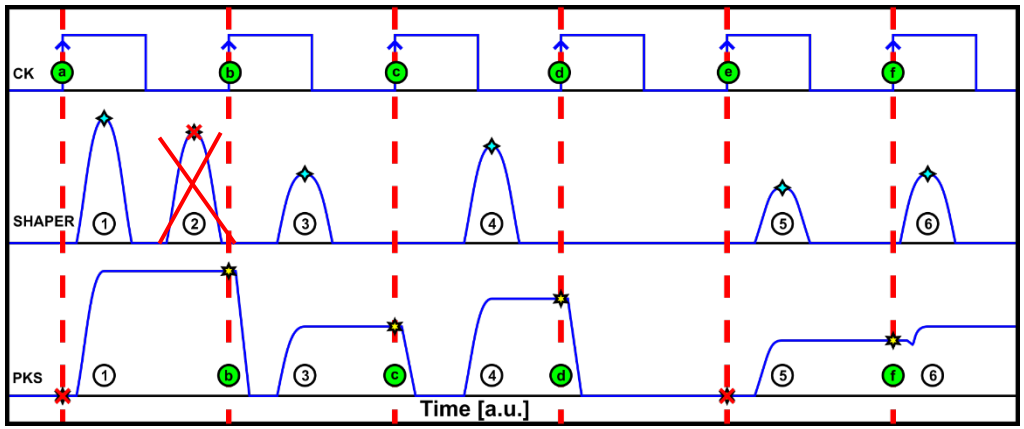
None acceptable

OCR limitation due to ADC sampling: → derandomization

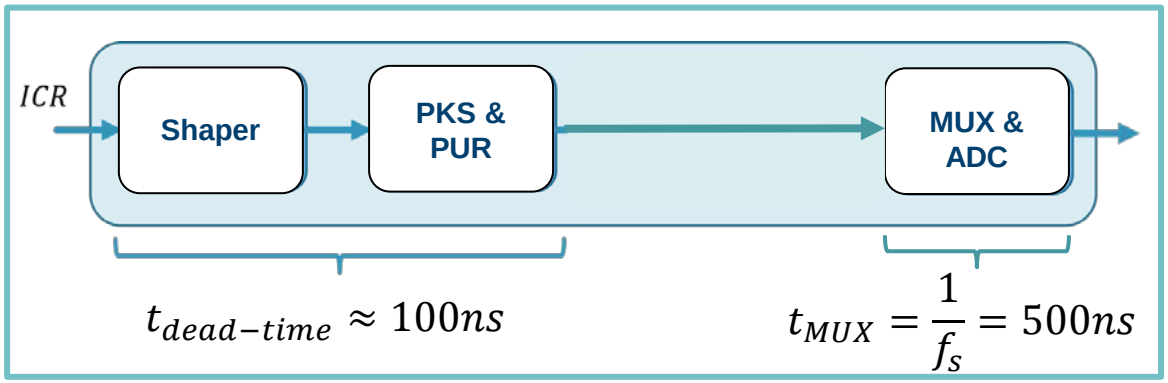


- Randomly distributed events are sampled with constant sampling frequency
- Some events are not sampled, some samples are wasted
- Different derandomization techniques possible (e.g. P.O'Connor, et al., IEEE TNS, 2003)

Finite Sampling Frequency

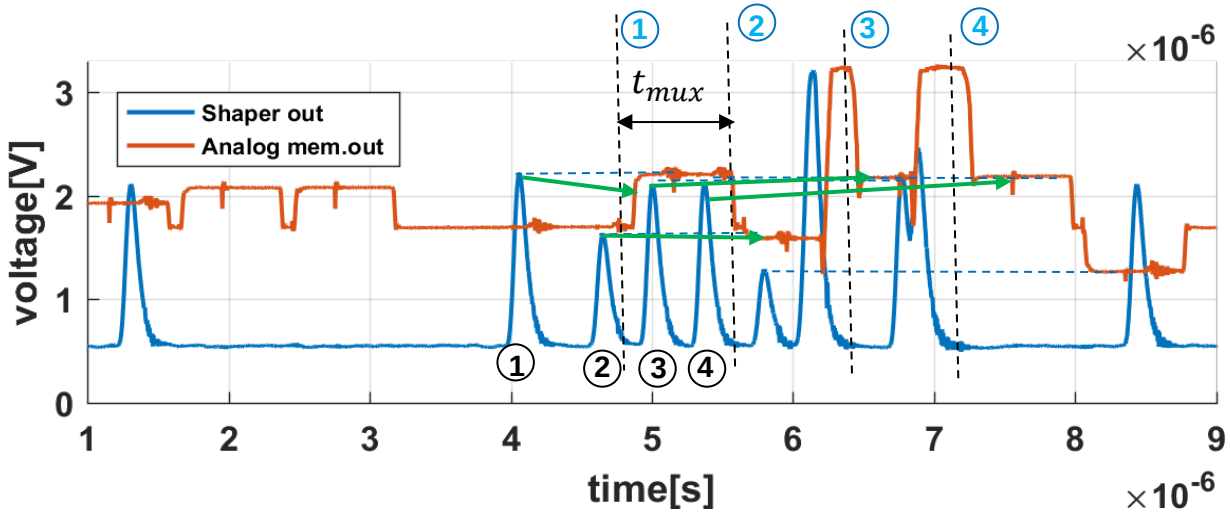


Derandomization by an Analog Memory



Memory cells **derandomize** the peak acquisition of pulses, allowing higher channel throughput.

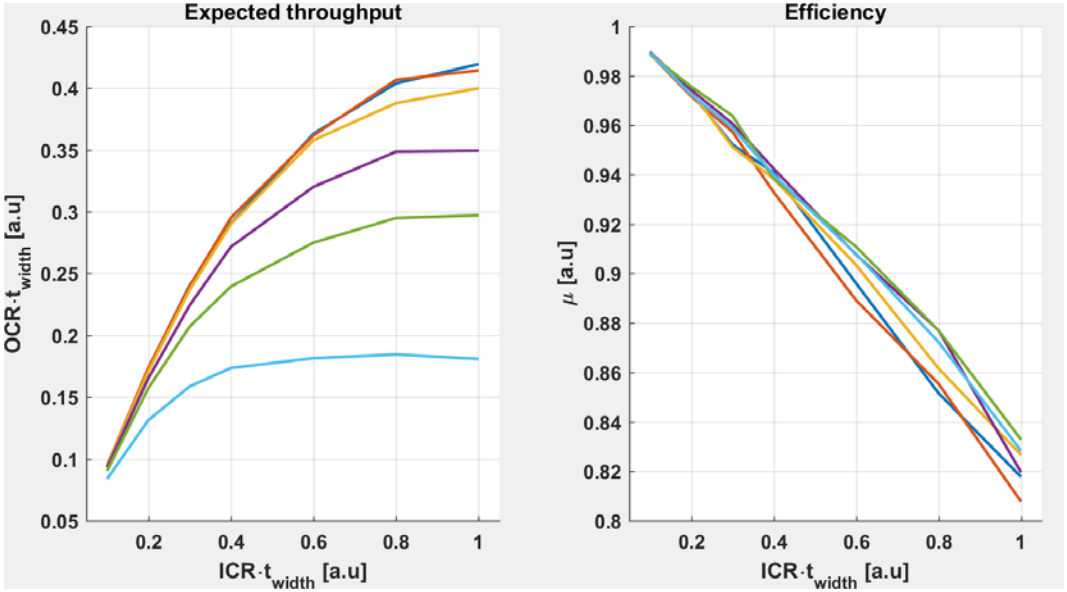
Measurements



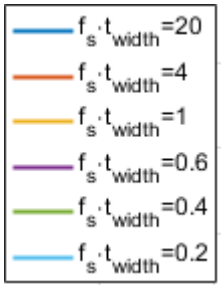
(TERA ASIC, Polimi)

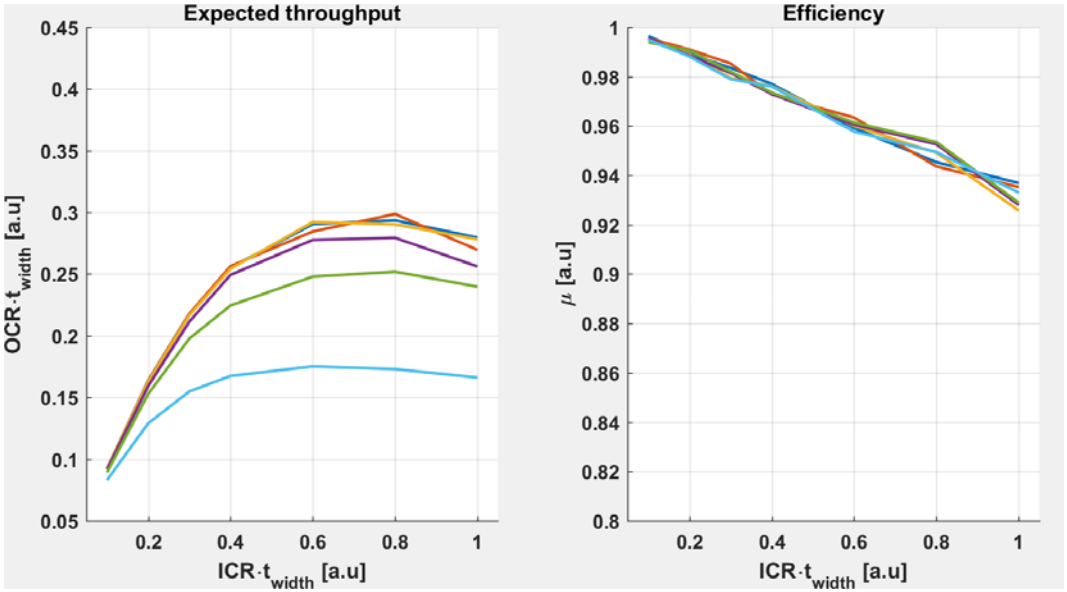
Comparison of PUR algorithms (with derandomization)

'delay' PUR



ADC sampling frequency



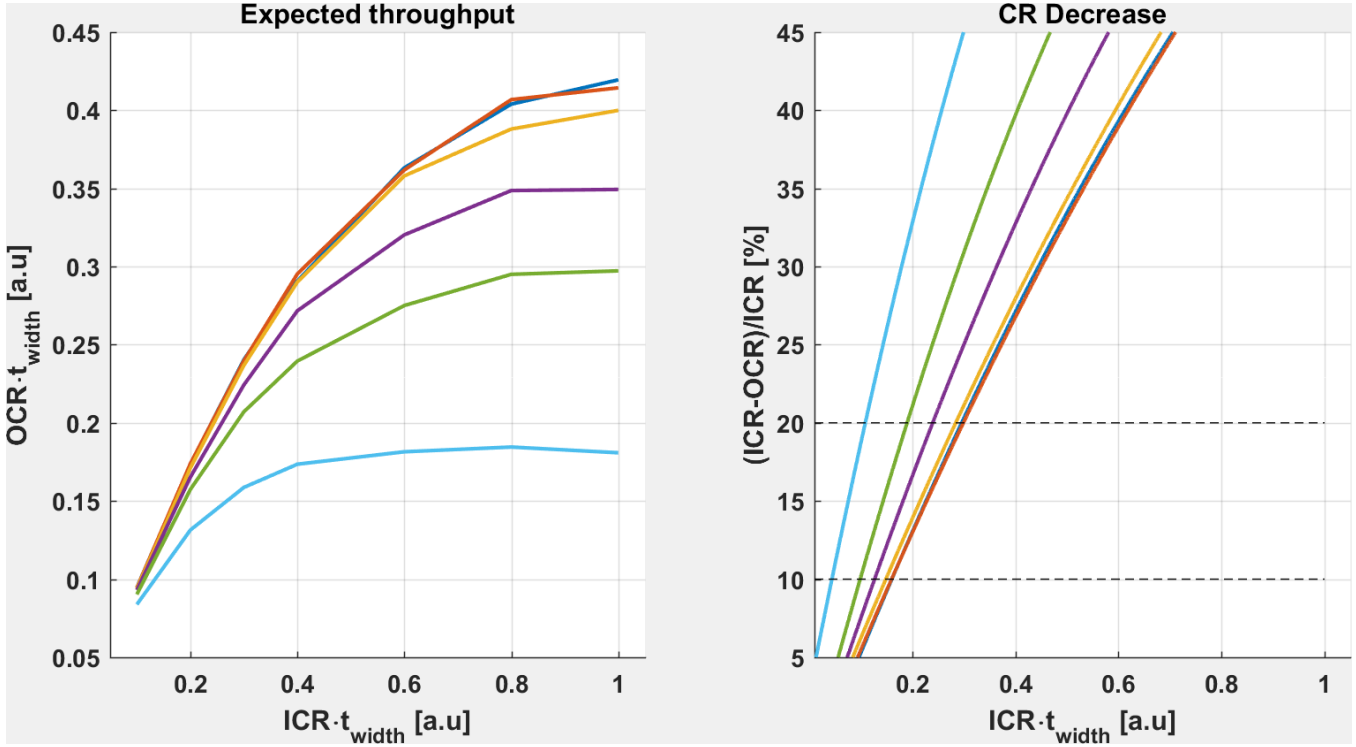


'rise' PUR

Figures of merit:

Throughput: ratio between Output Count Rate (OCR) and Input Count Rate (ICR)

Efficiency (i.e. quality): ratio between Good Pulses (amplitude error <1%) and Accepted Pulses



- SDD+CUBE
- analog shaping
- 200ns pulse width
- 155eV @6keV (11.6e- rms)
- 'delay' PUR

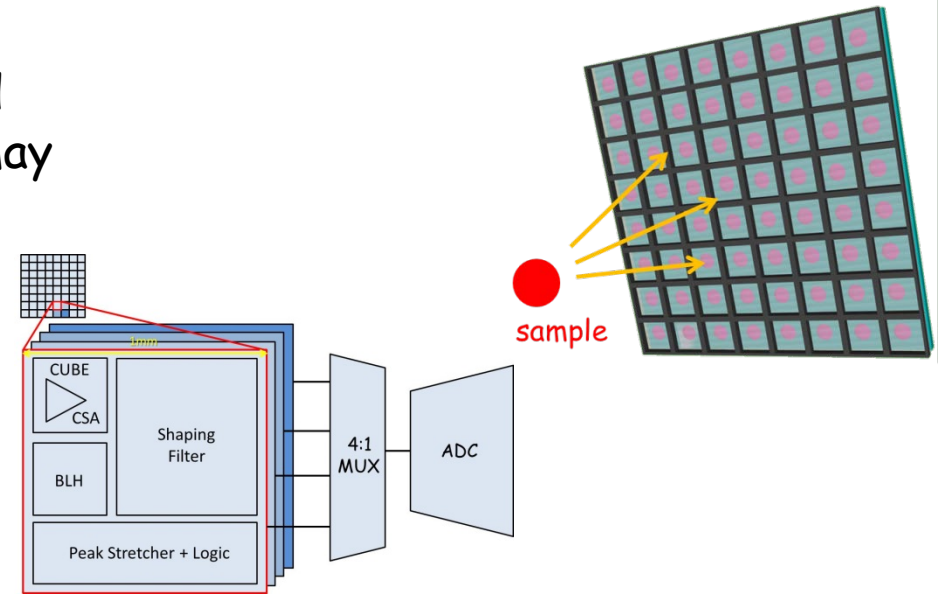
(simulations for TERA design, TERA: Throughput Enhanced Readout Asic, NSS 2017)

ADC fs (MHz)	ICRmax (Mcps)	OCRmax (Mcps)	OCR/ICR (%)
2	3	1,4	45
unlimited	3	1,8	60

ADC fs (MHz)	OCR@10%DT (Mcps)	OCR@20%DT (Mcps)
2	0,45	0,76
5	0,67	1,14
unlimited	0,72	1,18

Analog ASICs for X-ray spectroscopy: discussion

- Analog ASICs can provide good energy resolution and 0.5-1Mcps/ch count rate, although inferior to throughput capability of state-of-the-art digital processors
- Ultimate throughput takes into account minimum pulse duration for noise performances, ballistic deficit limitations and pile-rejection.
- Potential use still in highly integrated detector systems (with also direct digital output), e.g. from several tens to hundreds of channels (e.g. 100 channels detector @1Mcps/ch. → 100Mcps total throughput) and in systems with power, space and costs limitations (e.g. in some not-synchrotron applications…).
- Bump-bonded SDD-arrays based X-ray spectroscopy detectors may benefit of integration of full analog electronics chain (preamplifier+filter+ADC) in a single ASIC.



thank you for your attention!